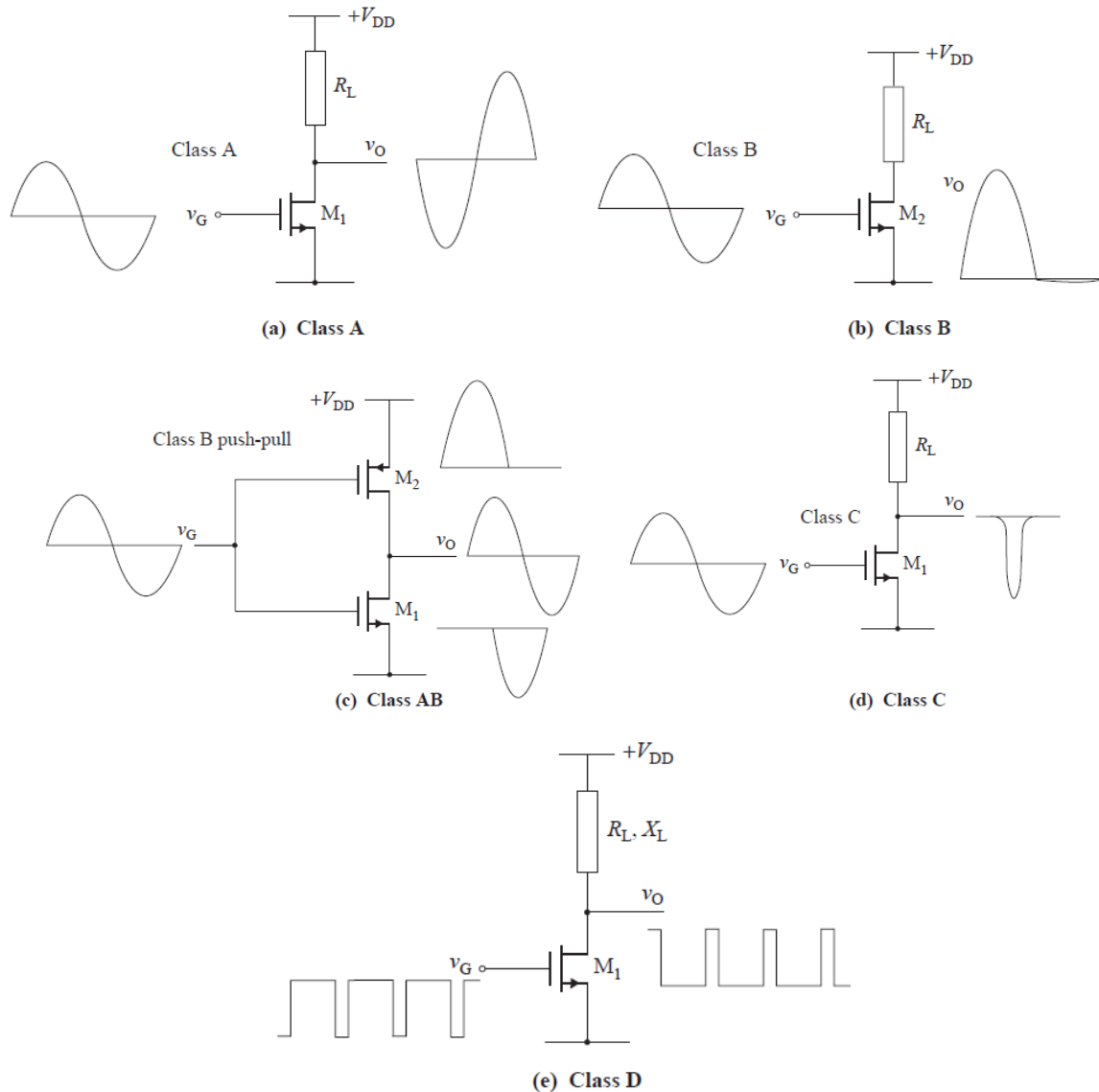# Power amplifiers

Classification of Power Amplifiers

Power amplifiers are generally classified into five types: A, B, AB, and C for analog designs and class D for switching designs. This classification is based on the percentage of the input cycle for which the amplifier operates in its **linear region**. The waveforms of the output currents for various types of amplifiers are shown in Fig. 1.

(a) Class A

(b) Class B

(c) Class AB

(d) Class C

(e) Class D

FIGURE 1 Output voltages for various classes of amplifiers

An amplifier receives a signal from input source and provides a larger version of the signal to some output device or to another amplifier stage. An input signal is generally small (a few microvolts from an antenna) and needs to be amplified sufficiently to operate an output device (speaker or other power-handling device).

Power amplifiers primarily provide sufficient power to an output load to drive a speaker or other power device, typically a few watts to tens of watts.

The main features of a power amplifier are the circuit's power efficiency, the maximum amount of power that the circuit is capable of handling, and the impedance matching to the output device.

Amplifier Efficiency

The power efficiency of an amplifier, defined as the ratio of power output to power input. In a class A amplifier, the maximum efficiency occurring for the largest output voltage and current swing (only 25% with a direct load connection and 50% with a transformer connection to the load). Class B operation, with no dc bias power for no input signal, can be shown to provide a maximum efficiency that reaches 78.5%. Class D operation can achieve power efficiency over 90% and provides the most efficient operation of all the operating classes. Since class AB falls between class A and class B in bias, it also falls between their efficiency ratings between 25% (or 50%) and 78.5%. Table-1 summarizes the operation of the various amplifier classes. This table provides a relative comparison of the output cycle operation and power efficiency for the various class types.

TABLE 1
Comparison of Amplifier Classes

Class	A	AB	B	C	D
Operating cycle	360°	180° to 360°	180°	Less than 180°	Pulse operation
Power efficiency	25% to 50%	Between 25% (50%) and 78.5%	78.5%		Typically over 90%

CLASS A AMPLIFIER

The simple circuit of a class A amplifier shown in Fig. 2. The signals handled by the circuit are in the range of volts, and the transistor used is a power transistor that is capable of operating in the range of a few to tens of watts. The circuit is not the best to use as a large-signal amplifier because of its poor power efficiency. **The beta of a power transistor is generally less than 100**,
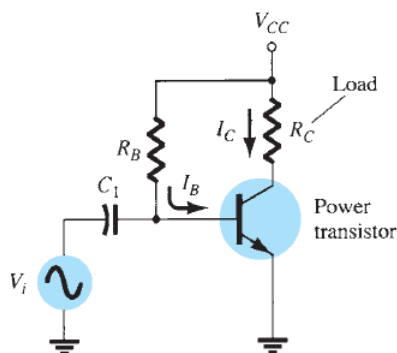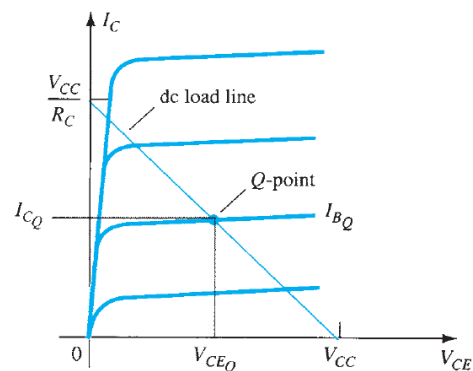

Fig. 2

Fig. 3

2

DC Bias Operation

The dc bias set by V_{CC} and R_B fixes the dc base-bias current at

$$I_B = \frac{V_{CC} - 0.7 \text{ V}}{R_B}$$

with the collector current then being

$$I_C = \beta I_B$$

with the collector–emitter voltage then

$$V_{CE} = V_{CC} - I_C R_C$$

To appreciate the importance of the dc bias on the operation of the power amplifier, consider the collector characteristic shown in Fig. 3 . **A dc load line is drawn using the values of V $_{CC}$ and R$_C$. The intersection of the dc bias value of I $_B$ with the dc load line then determines the operating point (Q -point) for the circuit. The quiescent-point values are those calculated using Eqs. (1) through (3). If the dc bias collector current is set at one-half the possible signal swing (between 0 and V $_{CC}/R_C$), the largest collector current swing will be possible. Additionally, if the quiescent collector–emitter voltage is set at one-half the supply voltage, the largest voltage swing will be possible (Q–point set at optimum bias point).**

AC Operation

When an input ac signal is applied to the amplifier of Fig. 2, the output will vary from its dc bias operating voltage and current. A small input signal, as shown in Fig. 4 , will cause the base current to vary above and below the dc bias point, which will then cause the collector current (output) to vary from the dc bias point set as well as the collector–emitter voltage to vary around its dc bias value. As the input signal is made larger, the output will vary further around the established dc bias point until either the current or the voltage reaches a limiting condition. **For the current this limiting condition is either zero current at the low end or V $_{CC}/R_C$ at the high end of its swing. For the collector–emitter voltage, the limit is either 0 V or the supply voltage, V_{CC}.**

Power Considerations

The power into an amplifier is provided by the supply voltage. With no input signal, the dc current drawn is the collector bias current I_{CQ}. The power then drawn from the supply is:

$$P_i(\text{dc}) = V_{CC} I_{C_Q}$$

Even with an ac signal applied, the average current drawn from the supply remains equal to the quiescent current I_{CQ}, so that Eq.(4) represents the input power supplied to the class A amplifier.
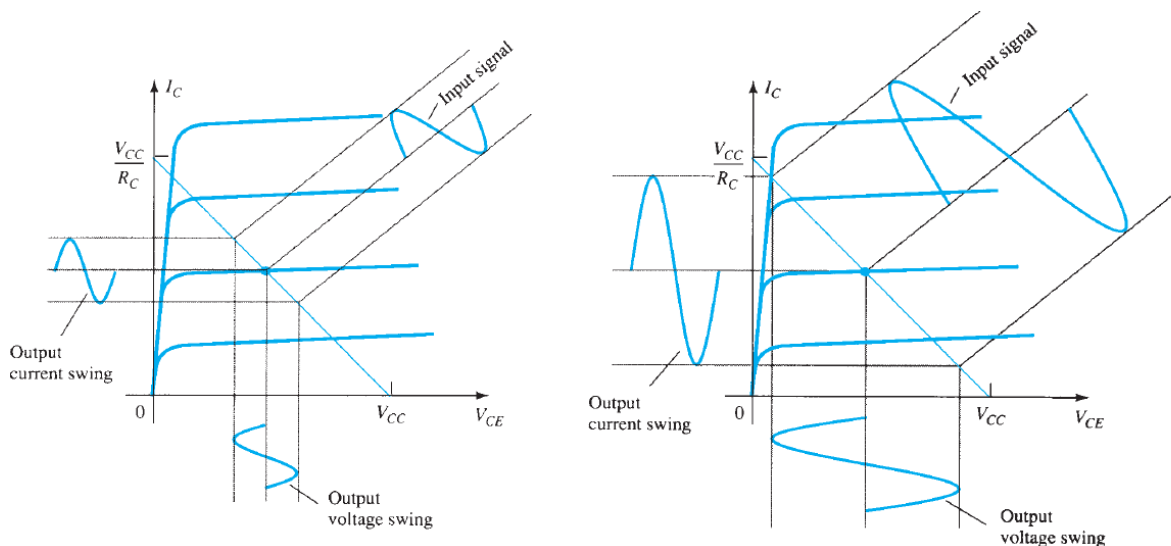
Fig. 4

Output Power

The output voltage and current varying around the bias point provide ac power to the load. This ac power is delivered to the load R_C in the circuit of Fig. 2. The ac signal Vi causes the base current to vary around the dc bias current and the collector current around its quiescent level I_{CQ}. As shown in Fig. 4 , the ac input signal results in ac current and ac voltage signals. The larger the input signal, the larger is the output swing, up to the maximum set by the circuit. The ac power delivered to the load (R_C) can be expressed in a number of ways.

The ac power delivered to the load (R_C) may be expressed using RMS signals

$$P_o(\text{ac}) = V_{CE}(\text{rms})I_C(\text{rms})$$

$$P_o(\text{ac}) = I_C^2(\text{rms})R_C$$

$$P_o(\text{ac}) = \frac{V_C^2(\text{rms})}{R_C}$$

Efficiency

The efficiency of an amplifier represents the amount of ac power delivered (transferred) from the dc source. The efficiency of the amplifier is calculated using

$$\% \, \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\%$$

Maximum Efficiency = 25% (This maximum efficiency will occur only for ideal conditions of both voltage swing and current swing, most of class A circuits will provide efficiencies of much less than 25%.)

EXAMPLE 1: Calculate the input power, output power, and efficiency of the amplifier circuit in Fig. 5 for an input voltage that results in a base current of 10 mA peak.
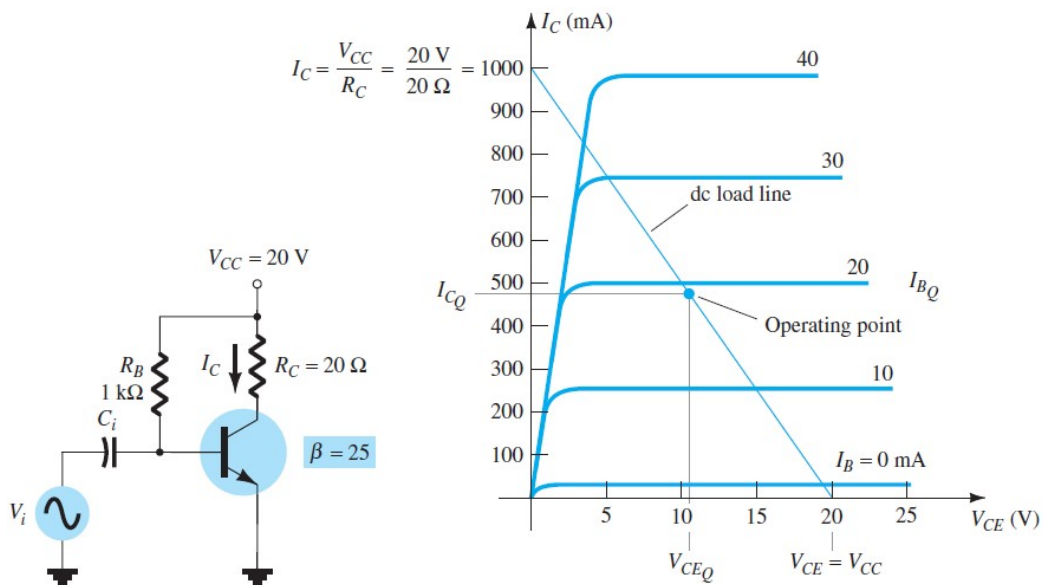
4

Fig.5

Solution:

$$I_{B_Q} = \frac{V_{CC} - 0.7\ V}{R_B} = \frac{20\ V - 0.7\ V}{1\ k\Omega} = 19.3\ mA$$

$$I_{C_Q} = \beta I_B = 25(19.3\ mA) = 482.5\ mA \cong 0.48\ A$$

$$V_{CE_Q} = V_{CC} - I_C R_C = 20\ V - (0.48\ \Omega)(20\ \Omega) = 10.4\ V$$

$$P_{dc} = I_{CQ} * V_{CC} = 0.48 * 20 = 9.6\ Watt$$

The ac variation of the output signal can be obtained graphically using the dc load line drawn on Fig. 4- b by connecting $V_{CE} = V_{CC} = 20\ V$ with $I_C = V_{CC}/R_C = 1000\ mA = 1\ A$

$$I_C(p) = \beta I_B(p) = 25(10\ mA\ peak) = 250\ mA\ peak$$
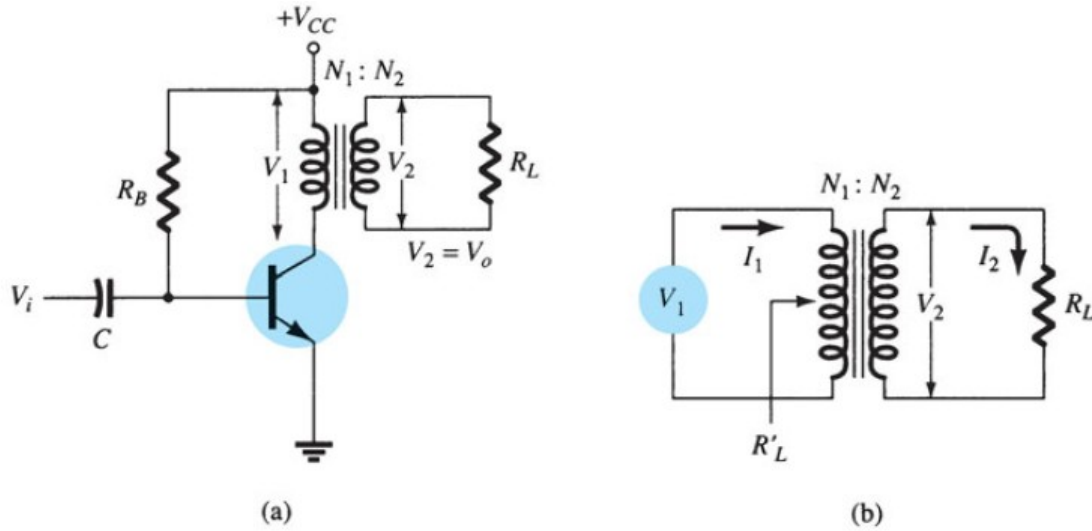
$$P_o(ac) = I_C^2(rms)R_C = \frac{I_C^2(p)}{2}R_C = \frac{(250 \times 10^{-3}\ A)^2}{2}(20\ \Omega) = \mathbf{0.625\ W}$$

$$\%\ \eta = \frac{P_o(ac)}{P_i(dc)} \times 100\% = \frac{0.625\ W}{9.6\ W} \times 100\% = \mathbf{6.5\%}$$

++

5

TRANSFORMER-COUPLED CLASS A AMPLIFIER

A form of class A amplifier having maximum efficiency of 50% uses a transformer to couple the output signal to the load as shown in a simple circuit of Fig. 6.

FIG. 6 *Transformer-coupled audio power amplifier.*

Transformer Action

A transformer can increase or decrease voltage or current levels according to the turns ratio. In the following discussion assumes ideal (100%) power transfer from primary to secondary, that is, no power losses are considered.

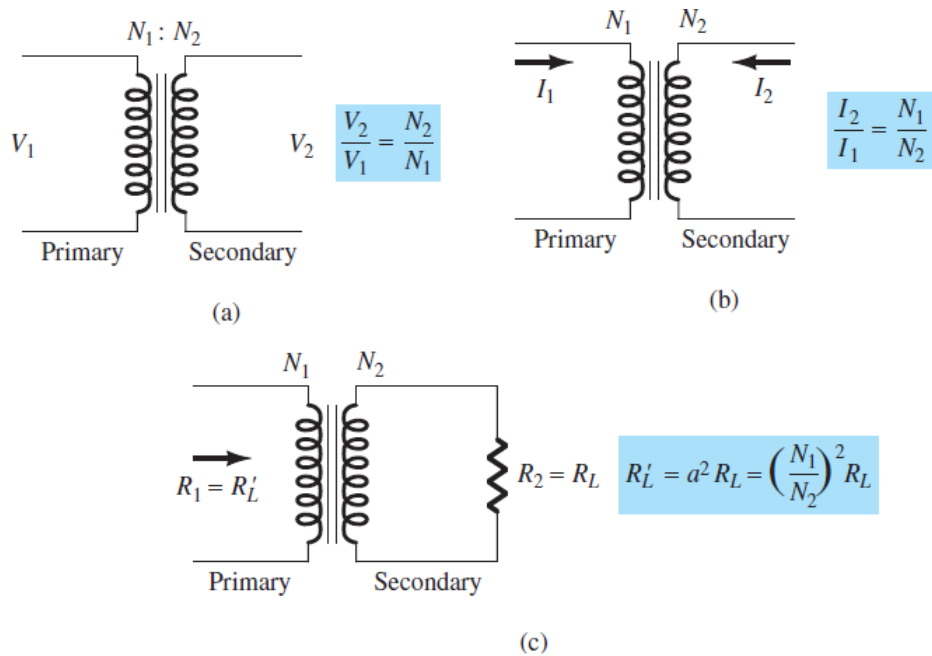**Voltage Transformation:** The voltage transformation is given by

$$\frac{V_2}{V_1} = \frac{N_2}{N_1}$$

Current Transformation: The current transformation is given by

$$\frac{I_2}{I_1} = \frac{N_1}{N_2}$$

Impedance Transformation: Since the voltage and current can be changed by a transformer, an impedance "seen" from either side (primary or secondary) can also be changed. As shown in Fig. 7- c, an impedance R_L is connected across the transformer secondary. This impedance is changed by the transformer when viewed at the primary side (R). This can be shown as follows:

$$\frac{R_L}{R'_L} = \frac{R_2}{R_1} = \frac{V_2/I_2}{V_1/I_1} = \frac{V_2 I_1}{I_2 V_1} = \frac{V_2 I_1}{V_1 I_2} = \frac{N_2 N_2}{N_1 N_1} = \left(\frac{N_2}{N_1}\right)^2$$

FIG.7: *(a) voltage transformation; (b) current transformation;(c) impedance transformation.*

If we define $a = N_1/N_2$, where a is the turns ratio of the transformer, the above equation becomes

$$\frac{R_L'}{R_L} = \frac{R_1}{R_2} = \left(\frac{N_1}{N_2}\right)^2 = a^2$$

We can express the load resistance reflected to the primary side as

$$R_1 = a^2 R_2 \quad \text{or} \quad R_L' = a^2 R_L$$

where R_L is the reflected impedance. As shown in Eq. , the reflected impedance is related directly to the square of the turns ratio. If the number of turns of the secondary is smaller than that of the primary, the impedance seen looking into the primary is larger than that of the secondary by the square of the turns ratio.

EXAMPLE 2: What transformer turns ratio is required to match a 16Ω speaker load so that the effective load resistance seen at the primary is 10 kΩ.

Solution:

$$\left(\frac{N_1}{N_2}\right)^2 = \frac{R_L'}{R_L} = \frac{10\,\text{k}\Omega}{16\,\Omega} = 625$$

$$\frac{N_1}{N_2} = \sqrt{625} = 25{:}1$$

Operation of Amplifier Stage

DC Load Line

The transformer (dc) winding resistance determines the dc load line for the circuit of Fig. 6. **Typically, this dc resistance is small (ideally 0Ω).** In Fig. 8, a **0 Ω dc load line is a straight**

vertical line. A practical transformer winding resistance would be a few ohms, but only the ideal case will be considered in this discussion.

There is no dc voltage drop across the 0Ω dc load resistance, and the load line is drawn straight vertically from the voltage point, $V_{CEQ} = V_{CC}$.
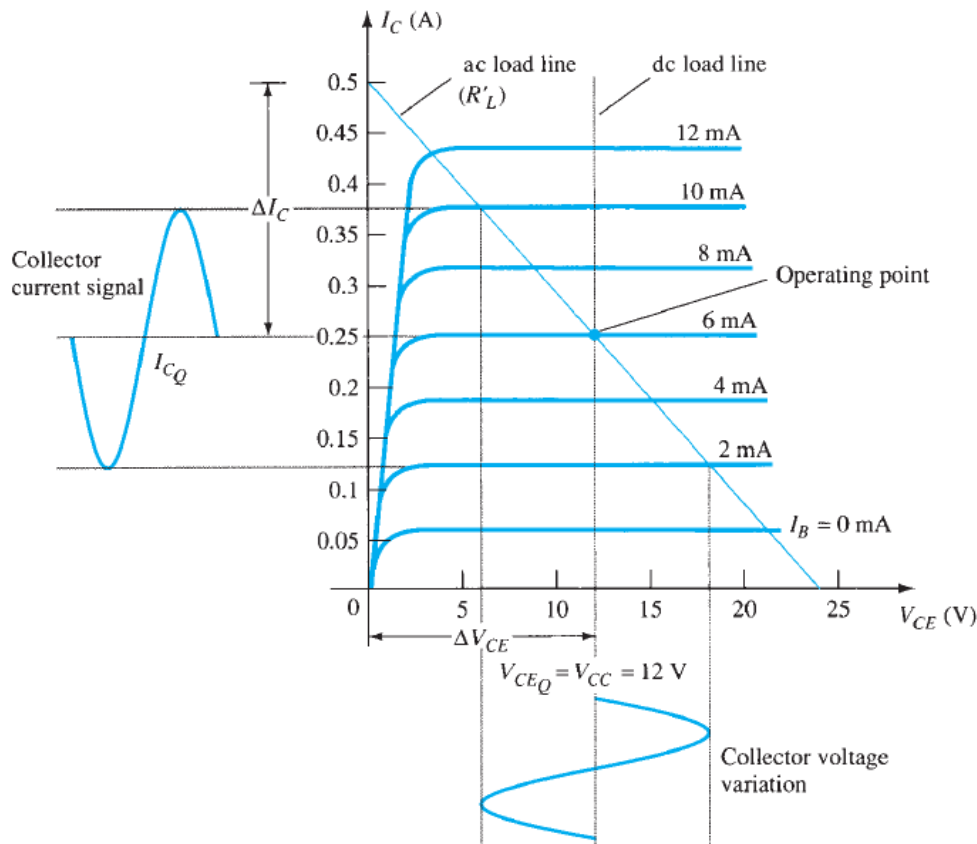
FIG. 8: *Load lines for class A transformer-coupled amplifier.*

Quiescent Operating Point

The operating point in the characteristic curve of Fig. 8 can be obtained graphically at the point of intersection of the dc load line and the base current set by the circuit. The collector quiescent current can then be obtained from the operating point. In class A operation, keep in mind that the dc bias point sets the conditions for the maximum undistorted signal swing for both collector current and collector–emitter voltage. If the input signal produces a voltage swing less than the maximum possible, the efficiency of the circuit at that time will be less than the maximum of 50%. The dc bias point is therefore important in setting the operation of a class A amplifier.

AC Load Line

To carry out ac analysis, it is necessary to calculate the ac load resistance "seen" looking into the primary side of the transformer, then draw the ac load line on the collector

characteristic. The reflected load resistance (R_L) is calculated using Eq.11 using the value of the load connected across the secondary (R) and the turns ratio of the transformer. The graphical analysis technique then proceeds as follows:

Draw the ac load line so that it passes through the operating point and has a slope equal to 1/R_L (the reflected load resistance), **the load line slope being the negative reciprocal of the ac load resistance**. **Notice that the ac load line shows that the output signal swing can exceed the value of V_{CC}. In fact, the voltage developed across the transformer primary can be quite large.** It is therefore necessary after obtaining the ac load line to check that the possible voltage swing does not exceed transistor maximum ratings.

Signal Swing and Output AC Power

Figure 9 shows the voltage and current signal swings from the circuit of Fig. 6 . From the signal variations shown in Fig. 8 , the values of the peak-to-peak signal swings are:

$$V_{CE}(\text{p-p}) = V_{CE_{max}} - V_{CE_{min}}$$
$$I_C(\text{p-p}) = I_{C_{max}} - I_{C_{min}}$$

(a) (b)
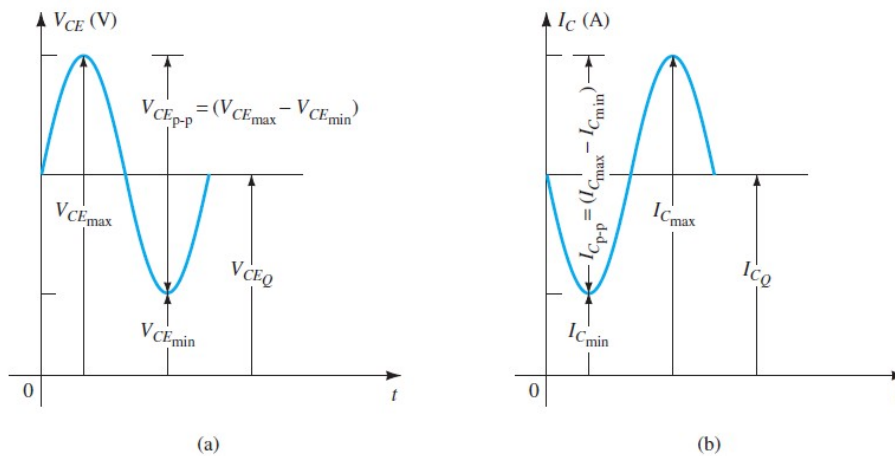
FIG. 9: *Graphical operation of transformer-coupled class A amplifier.*

The ac power developed across the transformer primary can then be calculated using:

$$P_o(\text{ac}) = \frac{(V_{CE_{max}} - V_{CE_{min}})(I_{C_{max}} - I_{C_{min}})}{8}$$

The ac power calculated is that developed across the primary of the transformer. Assuming an ideal transformer (a highly efficient transformer has an efficiency of well over 90%), we find that the power delivered by the secondary to the load is approximately that calculated using Eq. (13). The output ac power can also be determined using the voltage delivered to the load. For the ideal transformer, the voltage delivered to the load can be calculated using Eq. (7):

$$V_L = V_2 = \frac{N_2}{N_1}V_1$$

The power across the load can then be expressed as

$$P_L = \frac{V_L^2(\text{rms})}{R_L}$$

Using Eq. (8) to calculate the load current yields

$$I_L = I_2 = \frac{N_1}{N_2}I_C$$

with the output ac power then calculated using

$$P_L = I_L^2(\text{rms})R_L$$

Efficiency

The input (dc) power obtained from the supply is calculated from the supply dc voltage and the average power drawn from the supply:

$$P_i(\text{dc}) = V_{CC}I_{C_Q}$$

For the transformer-coupled amplifier, the power dissipated by the transformer is small (due to the small dc resistance of a coil) and will be ignored in the present calculations. Thus the only power loss considered here is that dissipated by the power transistor and calculated using

$$P_Q = P_i(\text{dc}) - P_o(\text{ac})$$

where P_Q **is the power dissipated as heat**. The amount of power dissipated by the transistor is the difference between that drawn from the dc supply (set by the bias point) and the amount delivered to the ac load. When the input signal is very small, with very little ac power delivered to the load, the maximum power is dissipated by the transistor. When the input signal is larger and power delivered to the load is larger, less power is dissipated by the transistor. In other words, the transistor of a class A amplifier has to work hardest (dissipate the most power) when the load is disconnected from the amplifier, and the transistor dissipates the least power when the load is drawing maximum power from the circuit.

EXAMPLE 3: Calculate the ac power delivered to the 8Ω speaker for the circuit of Fig. 10. The circuit component values result in a dc base current of 6 mA, and the input signal (Vi) results in a peak base current swing of 4 mA.
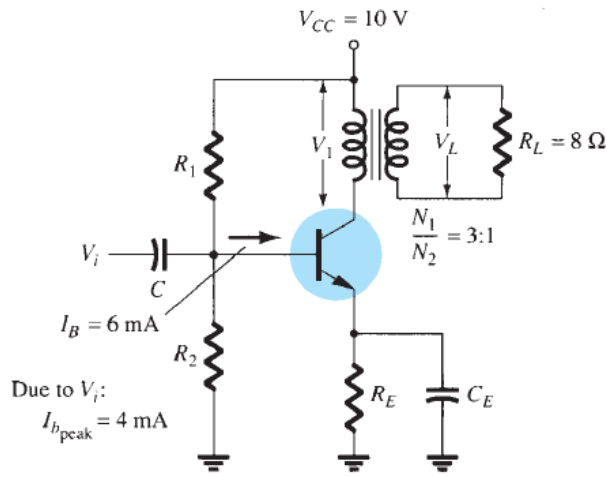
FIG. 10: *Transformer-coupled class A amplifier*

Solution: The dc load line is drawn vertically (see Fig. 11) from the voltage point:

$V_{CEQ} = V_{CC} = 10$ V

For $I_B = 6$ mA, the operating point on Fig. 10 is $V_{CEQ} = 10$ V and $I_{CQ} = 140$ mA

The effective ac resistance seen at the primary is

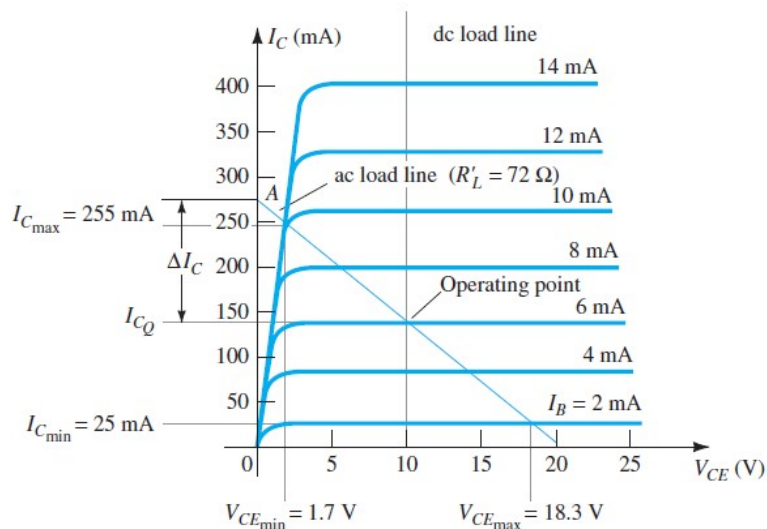$$R'_L = \left(\frac{N_1}{N_2}\right)^2 R_L = (3)^2(8) = 72 \ \Omega$$

The ac load line can then be drawn of slope -1/ 72 going through the indicated operating point.
To help draw the load line, consider the following procedure. For a current swing of

$$I_C = \frac{V_{CE}}{R'_L} = \frac{10 \text{ V}}{72 \ \Omega} = 139 \text{ mA}$$

mark a point A :

$$I_{CE_Q} + I_C = 140 \text{ mA} + 139 \text{ mA} = 279 \text{ mA along the y-axis}$$

(b)

FIG. 11: *Transformer-coupled class A transistor characteristic for Examples 3 and 4 :*
(a) device characteristic; (b) dc and ac load lines.

6

Connect point A through the Q-point to obtain the ac load line. For the given base current swing of 4 mA peak, the maximum and minimum collector current and collector–emitter voltage obtained from Fig. 10 are, respectively,

$$V_{CE_{min}} = 1.7 \text{ V} \qquad I_{C_{min}} = 25 \text{ mA}$$
$$V_{CE_{max}} = 18.3 \text{ V} \qquad I_{C_{max}} = 255 \text{ mA}$$

The ac power delivered to the load

$$P_o(\text{ac}) = \frac{(V_{CE_{max}} - V_{CE_{min}})(I_{C_{max}} - I_{C_{min}})}{8}$$

$$= \frac{(18.3 \text{ V} - 1.7 \text{ V})(255 \text{ mA} - 25 \text{ mA})}{8} = \mathbf{0.477 \text{ W}}$$

EXAMPLE 4: For the circuit of Fig. 10 and results of Example 3 , calculate the dc input power, power dissipated by the transistor, and efficiency of the circuit for the input signal of Example 3.

Solution:

$$P_i(\text{dc}) = V_{CC}I_{C_Q} = (10 \text{ V})(140 \text{ mA}) = \mathbf{1.4 \text{ W}}$$

$$P_Q = P_i(\text{dc}) - P_o(\text{ac}) = 1.4 \text{ W} - 0.477 \text{ W} = \mathbf{0.92 \text{ W}}$$

The efficiency of the amplifier is then

$$\% \, \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{0.477 \text{ W}}{1.4 \text{ W}} \times 100\% = \mathbf{34.1\%}$$

Maximum Theoretical Efficiency For a class A transformer-coupled amplifier, the maximum theoretical efficiency goes up to 50%.

EXAMPLE 5: Calculate the efficiency of a transformer-coupled class A amplifier for a supply of 12 V and outputs of:

a. $V_{(p)} = 12$ V, b. $V_{(p)} = 6$ V, c. $V_{(p)} = 2$ V

Solution:

a) Since $V_{CEQ} = V_{CC} = 12$ V, the maximum and minimum of the voltage swing are, respectively,

$$V_{CE_{max}} = V_{CE_Q} + V(\text{p}) = 12 \text{ V} + 12 \text{ V} = 24 \text{ V}$$
$$V_{CE_{min}} = V_{CE_Q} - V(\text{p}) = 12 \text{ V} - 12 \text{ V} = 0 \text{ V}$$

resulting in

$$\% \, \eta = 50\left(\frac{24 \text{ V} - 0 \text{ V}}{24 \text{ V} + 0 \text{ V}}\right)^2 \% = \mathbf{50\%}$$

b.

$$V_{CE_{max}} = V_{CE_Q} + V(p) = 12\text{ V} + 6\text{ V} = 18\text{ V}$$
$$V_{CE_{min}} = V_{CE_Q} - V(p) = 12\text{ V} - 6\text{ V} = 6\text{ V}$$

resulting in

$$\%\,\eta = 50\left(\frac{18\text{ V} - 6\text{ V}}{18\text{ V} + 6\text{ V}}\right)^2 \% = \mathbf{12.5\%}$$

c.

$$V_{CE_{max}} = V_{CE_Q} + V(p) = 12\text{ V} + 2\text{ V} = 14\text{ V}$$
$$V_{CE_{min}} = V_{CE_Q} - V(p) = 12\text{ V} - 2\text{ V} = 10\text{ V}$$

resulting in

$$\%\,\eta = 50\left(\frac{14\text{ V} - 10\text{ V}}{14\text{ V} + 10\text{ V}}\right)^2 \% = \mathbf{1.39\%}$$

Notice how dramatically the amplifier efficiency drops from a maximum of 50% for $V_{(p)} = V_{CC}$ to slightly over 1% for $V_{(p)} = 2$ V.

CLASS B AMPLIFIER OPERATION

In class B, the transistor turning on when the ac signal is applied. The transistor conducts current for only one-half of the signal cycle. To obtain output for the full cycle of signal, it is necessary to use two transistors and have each conduct on opposite half-cycles, the combined operation providing a full cycle of output signal. Since one part of the circuit pushes the signal high during one half-cycle and the other part pulls the signal low during the other half-cycle, the circuit is referred to as a *push–pull circuit*. Figure 11 shows a diagram for push–pull operation. An ac input signal is applied to the push–pull circuit, with each half operating on alternate half-cycles, the load then receiving a signal for the full ac cycle. The power transistors class B operation of these transistors provides greater efficiency than was possible using a single transistor in class A operation.
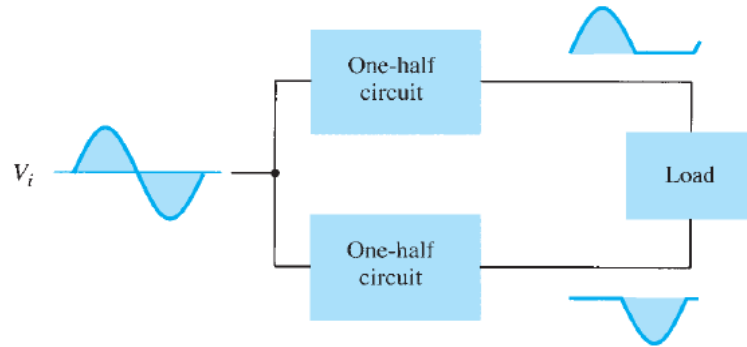
FIG. 11:*Block representation of push–pull operation.*

Input (DC) Power

The power supplied to the load by an amplifier is drawn from the power supply (see Fig. 12) that provides the input (or dc power). The amount of this input power can be calculated using:
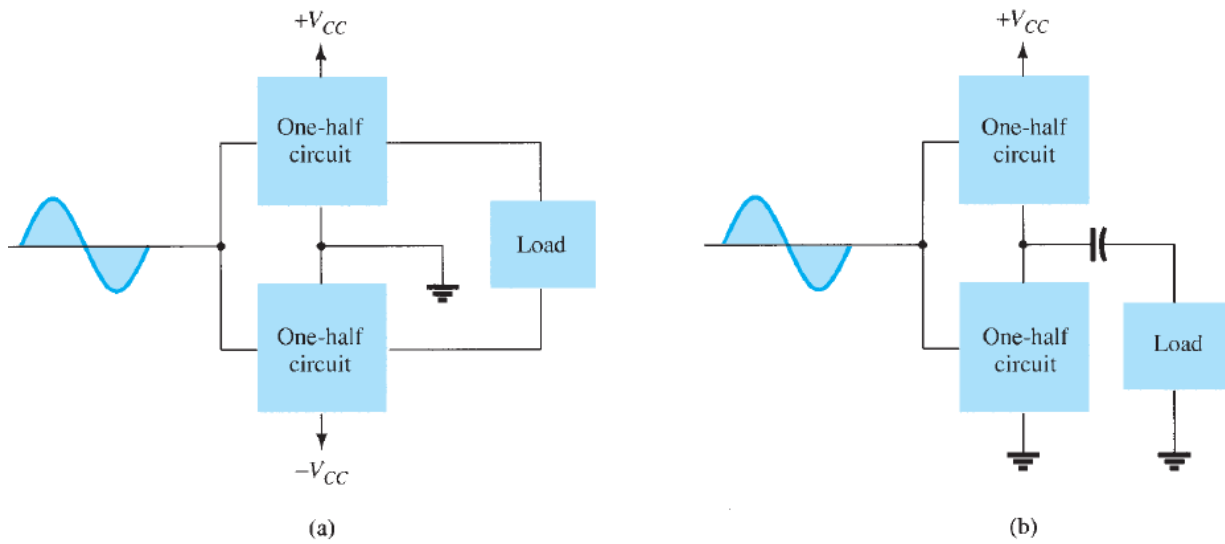
$$P_i(\text{dc}) = V_{CC}I_{\text{dc}} \qquad (1)$$

where I_{dc} is the average or dc current drawn from the power supplies. The value of the average current drawn can be expressed as

$$I_{\text{dc}} = \frac{2}{\pi}I(\text{p}) \qquad (2)$$

where $I_{(\text{p})}$ is the peak value of the output current waveform. Using Eq. (2) in the power input equation (1) results in

$$P_i(\text{dc}) = V_{CC}\left(\frac{2}{\pi}I(\text{p})\right) \qquad (3)$$

FIG.12: *Connection of push–pull amplifier to load: (a) using two voltage supplies; (b) using one voltage supply.*

Output (AC) Power

The power delivered to the load (usually referred to as a resistance R_L) can be calculated using any one of the following equations:

If one is using an rms meter to measure the voltage across the load, the output power can be calculated as:

$$P_o(\text{ac}) = \frac{V_L^2(\text{rms})}{R_L} \qquad (4)$$

If one is using an oscilloscope, the measured peak or peak-to-peak output voltage can be used:

$$P_o(\text{ac}) = \frac{V_L^2(\text{p-p})}{8R_L} = \frac{V_L^2(\text{p})}{2R_L} \qquad (5)$$

The larger the rms or peak output voltage, the larger is the power delivered to the load.

Efficiency

The efficiency of the class B amplifier can be calculated using the basic equation

$$\% \, \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% \qquad (6)$$

Using Eqs. (3) and (5) in the efficiency equation above results in

$$\% \, \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_L^2(\text{p})/2R_L}{V_{CC}[(2/\pi)I(\text{p})]} \times 100\% = \frac{\pi}{4} \frac{V_L(\text{p})}{V_{CC}} \times 100\% \qquad (7)$$

[using $I_{(\text{p})} = V_{L(\text{p})}/R_L$]. Equation (7) shows that the larger the peak voltage, the higher is the circuit efficiency, up to a maximum value when $V_{L(\text{p})} = VCC$, this maximum efficiency then being

$$\text{maximum efficiency} = \frac{\pi}{4} \times 100\% = 78.5\%$$

(8)

Power Dissipated by Output Transistors

The power dissipated (as heat) by the output power transistors is the difference between the input power delivered by the supplies and the output power delivered to the load,

$$P_{2Q} = P_{i(dc)} - P_{o(ac)}$$ **(9)**

where P_{2Q} is the power dissipated by the two output power transistors. The dissipated power handled by each transistor is then

$$PQ = P_{2Q} / 2$$ (10)

EXAMPLE 6: For a class B amplifier providing a 20-V peak signal to a 16Ω load (speaker) and a power supply of $V_{CC} = 30$ V, determine the input power, output power, *and circuit efficiency.*

Solution: A 20-V peak signal across a 16-Ω load provides a peak load current of

$$I_L(p) = \frac{V_L(p)}{R_L} = \frac{20 \text{ V}}{16 \text{ }\Omega} = 1.25 \text{ A}$$

The dc value of the current drawn from the power supply is then

$$I_{dc} = \frac{2}{\pi} I_L(p) = \frac{2}{\pi} (1.25 \text{ A}) = 0.796 \text{ A}$$

and the input power delivered by the supply voltage is

$$P_i(dc) = V_{CC} I_{dc} = (30 \text{ V})(0.796 \text{ A}) = \textbf{23.9 W}$$

The output power delivered to the load is

$$P_o(ac) = \frac{V_L^2(p)}{2R_L} = \frac{(20 \text{ V})^2}{2(16 \text{ }\Omega)} = \textbf{12.5 W}$$

for a resulting efficiency of

$$\% \eta = \frac{P_o(ac)}{P_i(dc)} \times 100\% = \frac{12.5 \text{ W}}{23.9 \text{ W}} \times 100\% = \textbf{52.3\%}$$

Maximum Power Considerations

For class B operation, the maximum output power is delivered to the load when

$$V_{L(p)} = V_{CC}$$ (11)

$$\text{maximum } P_o(ac) = \frac{V_{CC}^2}{2R_L}$$ (12)

The corresponding peak ac current $I(p)$ is then

$$I(\text{p}) = \frac{V_{CC}}{R_L} \qquad (13)$$

so that the maximum value of average current from the power supply is

$$\text{maximum } I_{dc} = \frac{2}{\pi}I(\text{p}) = \frac{2V_{CC}}{\pi R_L} \qquad (14)$$

Using this current to calculate the maximum value of input power results in

$$\text{maximum } P_i(\text{dc}) = V_{CC}(\text{maximum } I_{dc}) = V_{CC}\left(\frac{2V_{CC}}{\pi R_L}\right) = \frac{2V_{CC}^2}{\pi R_L} \qquad (15)$$

The maximum circuit efficiency for class B operation is then

$$\text{maximum } \% \, \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{V_{CC}^2/2R_L}{V_{CC}[(2/\pi)(V_{CC}/R_L)]} \times 100\%$$

$$= \frac{\pi}{4} \times 100\% = \textbf{78.54\%}$$

When the input signal results in less than the maximum output signal swing, the circuit efficiency is less than 78.5%.

For class B operation, the maximum power dissipated by the output transistors does not occur at the maximum power input or output condition. The maximum power dissipated by the two output transistors occurs when the output voltage across the load is

$$V_L(\text{p}) = 0.636V_{CC} \qquad \left(= \frac{2}{\pi}V_{CC}\right)$$

for a maximum transistor power dissipation of

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L}$$

EXAMPLE 7: For a class B amplifier using a supply of $V_{CC} = 30$ V and driving a load of 16Ω, determine the maximum input power, output power, and transistor dissipation.

Solution: The maximum output power is

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} = \frac{(30 \text{ V})^2}{2(16 \text{ }\Omega)} = \textbf{28.125 W}$$

The maximum input power drawn from the voltage supply is

$$\text{maximum } P_i(\text{dc}) = \frac{2V_{CC}^2}{\pi RL} = \frac{2(30 \text{ V})^2}{\pi(16 \text{ }\Omega)} = \textbf{35.81 W}$$

The circuit efficiency is then

$$\text{maximum } \% \, \eta = \frac{P_o(\text{ac})}{P_i(\text{dc})} \times 100\% = \frac{28.125 \text{ W}}{35.81 \text{ W}} \times 100\% = \textbf{78.54\%}$$

as expected. The maximum power dissipated by each transistor is

$$\text{maximum } P_Q = \frac{\text{maximum } P_{2Q}}{2} = 0.5\left(\frac{2V_{CC}^2}{\pi^2 R_L}\right) = 0.5\left[\frac{2(30 \text{ V})^2}{\pi^2 16 \text{ }\Omega}\right] = \textbf{5.7 W}$$

Under maximum conditions a pair of transistors each handling 5.7 W at most can deliver 28.125 W to a 16-Ω load while drawing 35.81 W from the supply.

The maximum efficiency of a class B amplifier can also be expressed as follows:

$$P_o(ac) = \frac{V_L^2(p)}{2R_L}$$

$$P_i(dc) = V_{CC}I_{dc} = V_{CC}\left[\frac{2V_L(p)}{\pi R_L}\right]$$

so that

$$\% \, \eta = \frac{P_o(ac)}{P_i(dc)} \times 100\% = \frac{V_L^2(p)/2R_L}{V_{CC}[(2/\pi)(V_L(p)/R_L)]} \times 100\%$$

$$\% \, \eta = 78.54\frac{V_L(p)}{V_{CC}}\%$$

EXAMPLE 8: Calculate the efficiency of a class B amplifier for a supply voltage of $V_{CC} = 24V$ with peak output voltages of: a. $V_{L(p)} = 22$ V. b. $V_{L(p)} = 6$ V.

Solution:

a. $\% \, \eta = 78.54\frac{V_L(p)}{V_{CC}}\% = 78.54\left(\frac{22 \text{ V}}{24 \text{ V}}\right) = \textbf{72\%}$

b. $\% \, \eta = 78.54\left(\frac{6 \text{ V}}{24 \text{ V}}\right)\% = \textbf{19.6\%}$

Notice that a voltage near the maximum [22V in part (a)] results in an efficiency near the maximum, whereas a small voltage swing [6V in part (b)] still provides an efficiency near 20%. Similar power supply and signal swings would have resulted in much poorer efficiency in a class A amplifier.

CLASS B AMPLIFIER CIRCUITS

A number of circuit arrangements for obtaining class B operation are possible. There are two common approaches for using push-pull amplifiers to reproduce the entire waveform. The first approach uses transformer coupling. The second uses two **complementary symmetry transistors** (*npn* and *pnp* , or *n*MOS and *p*MOS).

1- Transformer-Coupled Push–Pull Circuits

Transformer coupling is illustrated in Figure 13. The input transformer has a center-tapped secondary that is connected to ground, producing phase inversion of one side with respect to the other. The input transformer thus converts the input signal to two out-of-phase signals for the transistors. Notice that both transistors are *npn* types. Because of the signal inversion, $Q1$ will conduct on the positive part of the cycle and $Q2$ will conduct on the negative part. The overall

signal developed across the load then varies over the full cycle of signal operation. The positive power supply signal is connected to the center tap of the output transformer.
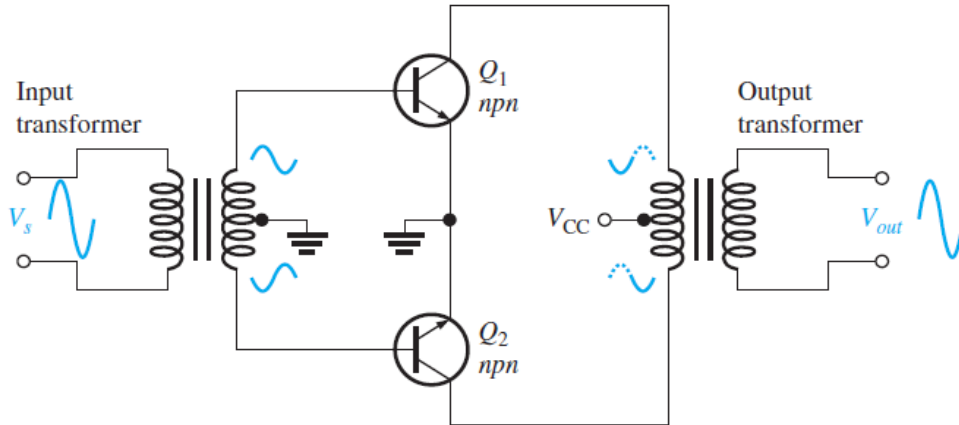
FIG. 13: *Transformer-coupled push-pull amplifiers. Q1 conducts during the positive half-cycle; Q2 conducts during the negative half-cycle. The two halves are combined by the output transformer.*

2- Complementary-Symmetry Circuits

Using complementary transistors (*npn* and *pnp*) it is possible to obtain a full cycle output across a load using half-cycles of operation from each transistor, as shown in Fig. 14-a. Whereas a single input signal is applied to the base of both transistors, the transistors, being of opposite type, will conduct on opposite half-cycles of the input. The *npn* transistor will be biased into conduction by the positive half-cycle of signal, with a resulting half cycle of signal across the load as shown in Fig. 14-b. During the negative half-cycle of signal, the *pnp* transistor is biased into conduction when the input goes negative, as shown in Fig. 14-c. During a complete cycle of the input, a complete cycle of output signal is developed across the load.
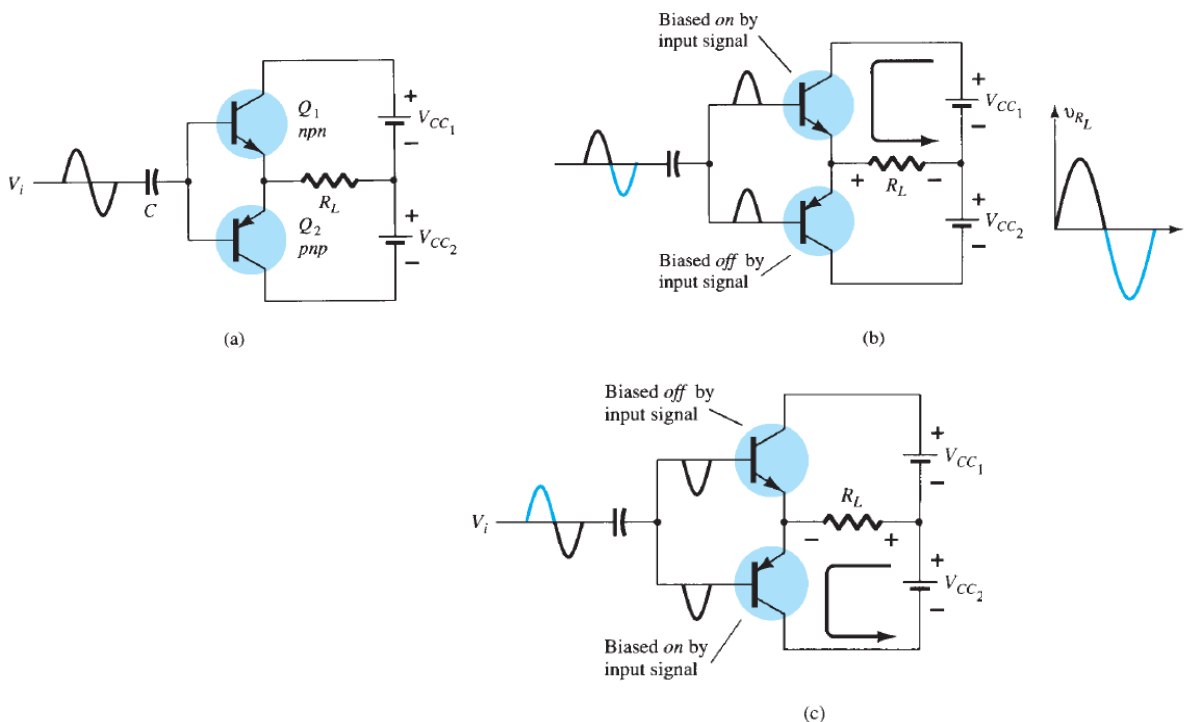
FIG. 14: *Complementary-symmetry push–pull circuit.*

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Crossover Distortion

When the dc base voltage is zero, both transistors are off and the input signal voltage must exceed V_{BE} before a transistor conducts. Because of this, there is a time interval between the positive and negative alternations of the input when neither transistor is conducting, as shown in Figure 15. The resulting distortion in the output waveform is called **crossover distortion.** Biasing the transistors in class AB improves this operation by biasing both transistors to be on for more than half a cycle.
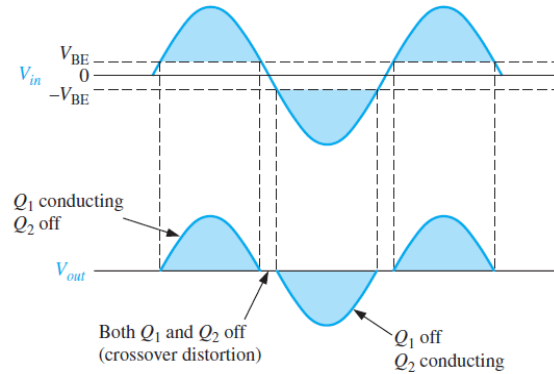
FIG.15: Illustration of crossover distortion in a class B push-pull amplifier. The transistors conduct only during portions of the input indicated by the shaded areas.

Biasing the Push-Pull Amplifier for Class AB Operation

To overcome crossover distortion, the biasing is adjusted to just overcome the V_{BE} of the transistors; this results in a modified form of operation called **class AB**. In class AB operation, the push-pull stages are biased into slight conduction, even when no input signal is present. This can be done with a voltage-divider and diode arrangement, as shown in Figure 16. When the diode characteristics of $D1$ and $D2$ are closely matched to the characteristics of the transistor base-emitter junctions, the current in the diodes and the current in the transistors are the same; this is called a **current mirror.** This current mirror produces the desired class AB operation and eliminates crossover distortion.
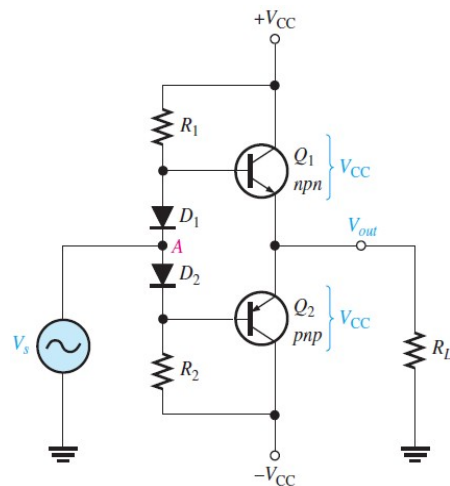
Fig. 16

In the bias path of the circuit in Figure 16, $R1$ and $R2$ are of equal value, as are the positive and negative supply voltages. This forces the voltage at point A (between the diodes) to equal 0 V and eliminates the need for an input coupling capacitor. The dc voltage on the output is also 0V. Assuming that both diodes and both complementary transistors are identical, the drop across $D1$ equals the V_{BE} of $Q1$, and the drop across $D2$ equals the V_{BE} of $Q2$.

EXAMPLE 9: For the circuit of Fig. 17 , calculate the input power, output power, power handled by each output transistor and the circuit efficiency for an input of 12 V rms.(assume voltage gain unity)
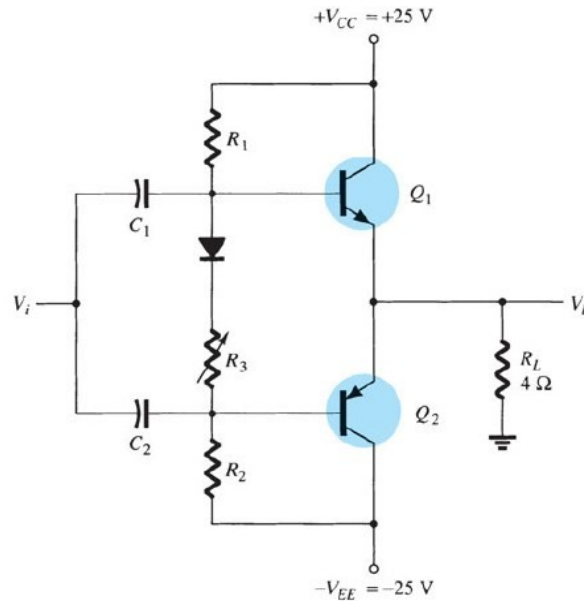
FIG. 17: *Class B power amplifier for Examples 9 to 11 .*

Solution: The peak input voltage is
$$V_i(\text{p}) = \sqrt{2}\, V_i\,(\text{rms}) = \sqrt{2}\,(12\text{ V}) = 16.97\text{ V} \approx 17\text{ V}$$
Since the resulting voltage across the load is ideally the same as the input signal (the amplifier has, ideally, a voltage gain of unity),
$$V_L(\text{p}) = 17\text{ V}$$
and the output power developed across the load is
$$P_o(\text{ac}) = \frac{V_L^2(\text{p})}{2R_L} = \frac{(17\text{ V})^2}{2(4\,\Omega)} = \textbf{36.125 W}$$

The peak load current is
$$I_L(\text{p}) = \frac{V_L(\text{p})}{R_L} = \frac{17\text{ V}}{4\,\Omega} = 4.25\text{ A}$$
from which the dc current from the supplies is calculated to be
$$I_{dc} = \frac{2}{\pi}I_L(\text{p}) = \frac{2(4.25\text{ A})}{\pi} = 2.71\text{ A}$$

so that the power supplied to the circuit is
$$P_i(\text{dc}) = V_{CC}I_{dc} = (25\text{ V})(2.71\text{ A}) = \textbf{67.75 W}$$
The power dissipated by each output transistor is
$$P_Q = \frac{P_{2Q}}{2} = \frac{P_i - P_o}{2} = \frac{67.75\text{ W} - 36.125\text{ W}}{2} = \textbf{15.8 W}$$

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The circuit efficiency (for the input of 12 V, rms) is then

$$\% \, \eta = \frac{P_o}{P_i} \times 100\% = \frac{36.125 \text{ W}}{67.75 \text{ W}} \times 100\% = \mathbf{53.3\%}$$

EXAMPLE 10: For the circuit of Fig. 17 , calculate the maximum input power, maximum output power, input voltage for maximum power operation, and power dissipated by the output transistors at this voltage.

Solution: The maximum input power is

$$\text{maximum } P_i(\text{dc}) = \frac{2V_{CC}^2}{\pi R_L} = \frac{2(25 \text{ V})^2}{\pi 4 \, \Omega} = \mathbf{99.47 \text{ W}}$$

The maximum output power is

$$\text{maximum } P_o(\text{ac}) = \frac{V_{CC}^2}{2R_L} = \frac{(25 \text{ V})^2}{2(4 \, \Omega)} = \mathbf{78.125 \text{ W}}$$

[Note that the maximum efficiency is achieved:

$$\% \, \eta = \frac{P_o}{P_i} \times 100\% = \frac{78.125 \text{ W}}{99.47 \text{ W}} 100\% = \mathbf{78.54\%}]$$

To achieve maximum power operation the output voltage must be

$$V_L(\text{p}) = V_{CC} = 25 \text{ V}$$

and the power dissipated by the output transistors is then

$$P_{2Q} = P_i - P_o = 99.47 \text{ W} - 78.125 \text{ W} = \mathbf{21.3 \text{ W}}$$

EXAMPLE 11: For the circuit of Fig. 17 , determine the maximum power dissipated by the output transistors and the input voltage at which this occurs.

Solution: The maximum power dissipated by both output transistors is

$$\text{maximum } P_{2Q} = \frac{2V_{CC}^2}{\pi^2 R_L} = \frac{2(25 \text{ V})^2}{\pi^2 4 \, \Omega} = \mathbf{31.66 \text{ W}}$$

This maximum dissipation occurs at

$$V_L = 0.636 V_L(\text{p}) = 0.636(25 \text{ V}) = \mathbf{15.9 \text{ V}}$$

(Notice that at $V_L = 15.9$ V the circuit required the output transistors to dissipate 31.66 W, whereas at $V_L = 25$ V they only had to dissipate 21.3 W.)

AMPLIFIER DISTORTION

A pure sinusoidal signal has a single frequency at which the voltage varies positive and negative by equal amounts. Any signal varying over less than the full 360° cycle is considered to have distortion. An ideal amplifier is capable of amplifying a pure sinusoidal signal to provide a larger version, the resulting waveform being a pure single-frequency sinusoidal signal. When distortion occurs, the output will not be an exact duplicate (except for magnitude)

of the input signal.

Distortion can occur because the device characteristic is not linear, in which case nonlinear or amplitude distortion occurs. This can occur with all classes of amplifier operation. Distortion can also occur because the circuit elements and devices respond to the input signal differently at various frequencies, this being frequency distortion.

One technique for describing distorted but period waveforms uses Fourier analysis, a method that describes any periodic waveform in terms of its fundamental frequency component and frequency components at integer multiples these components are called *harmonic components* or *harmonics.* For example, a signal that is originally 1000 Hz could result, after distortion, in a frequency component at 1000Hz (1 kHz) and harmonic components at 2 kHz (2*1 kHz), 3kHz (3*1 kHz), 4 kHz (4*1kHz), and so on. The original frequency of 1 kHz is called the *fundamental frequency* ; those at integer multiples are the *harmonics* . The 2-kHz component is therefore called a *second harmonic* , that at 3 kHz is the *third harmonic* , and so on. The fundamental frequency is not considered a harmonic. Fourier analysis does not allow for fractional harmonic frequencies only integer multiples of the fundamental.

Harmonic Distortion

A signal is considered to have harmonic distortion when there are harmonic frequency components (not just the fundamental component). If the fundamental frequency has an amplitude A_1 and the nth frequency component has an amplitude A_n, a harmonic distortion can be defined as

$$\% \, n\text{th harmonic distortion} = \% \, D_n = \frac{|A_n|}{|A_1|} \times 100\%$$

The fundamental component is typically larger than any harmonic component.

EXAMPLE 12: Calculate the harmonic distortion components for an output signal having fundamental amplitude of 2.5 V, second harmonic amplitude of 0.25 V, third harmonic amplitude of 0.1 V, and fourth harmonic amplitude of 0.05 V.

Solution:

$$\% \, D_2 = \frac{|A_2|}{|A_1|} \times 100\% = \frac{0.25 \text{ V}}{2.5 \text{ V}} \times 100\% = \mathbf{10\%}$$

$$\% \, D_3 = \frac{|A_3|}{|A_1|} \times 100\% = \frac{0.1 \text{ V}}{2.5 \text{ V}} \times 100\% = \mathbf{4\%}$$

$$\% \, D_4 = \frac{|A_4|}{|A_1|} \times 100\% = \frac{0.05 \text{ V}}{2.5 \text{ V}} \times 100\% = \mathbf{2\%}$$

Total Harmonic Distortion

When an output signal has a number of individual harmonic distortion components, the signal can be seen to have a total harmonic distortion based on the individual elements as combined by the relationship of the following equation:

$$\% \text{ THD} = \sqrt{D_2^2 + D_3^2 + D_4^2 + \cdots} \times 100\%$$

where THD is total harmonic distortion.

EXAMPLE 13: Calculate the total harmonic distortion for the amplitude components given in Example 12.

Solution: Using the computed values of $D_2 = 0.10, D_3 = 0.04$, and $D_4 = 0.02$

$$\begin{aligned}
\% \text{ THD} &= \sqrt{D_2^2 + D_3^2 + D_4^2} \times 100\% \\
&= \sqrt{(0.10)^2 + (0.04)^2 + (0.02)^2} \times 100\% = 0.1095 \times 100\% \\
&= \mathbf{10.95\%}
\end{aligned}$$

An instrument such as a spectrum analyzer would allow measurement of the harmonics present in the signal by providing a display of the fundamental component of a signal and a number of its harmonics on a display screen. Similarly, a wave analyzer instrument allows more precise measurement of the harmonic components of a distorted signal by filtering out each of these components and providing a reading of these components. In any case, the technique of considering any distorted signal as containing a fundamental component and harmonic components is practical and useful. For a signal occurring in class AB or class B, the distortion may be mainly even harmonics, of which the second harmonic component is the largest. Thus, although the distorted signal theoretically contains all harmonic components from the second harmonic up, the most important in terms of the amount of distortion in the classes presented above is the second harmonic.

+++

CLASS C AND CLASS D AMPLIFIERS

Although class A, class AB, and class B amplifiers are most used as power amplifiers, class D amplifiers are popular because of their very high efficiency. Class C amplifiers, although not used as audio amplifiers, do find use in tuned circuits as in communications.

Class C Amplifier

A class C amplifier, such as that shown in Fig. 18, is biased to operate for less than 180° of the input signal cycle. The tuned circuit in the output, however, will provide a full cycle of output

signal for the fundamental or resonant frequency of the tuned circuit (L and C tank circuit) of the output. This type of operation is therefore limited to use at one fixed frequency, as occurs in a communications circuit, for example. Operation of a class C circuit is not intended primarily for large-signal or power amplifiers.
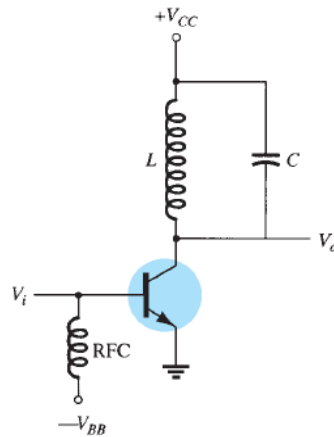
FIG. 18: *Class C amplifier circuit.*

Class D Amplifier

A class D amplifier is designed to operate with digital or pulse-type signals. An efficiency of over 90% is achieved using this type of circuit, making it quite desirable in power amplifiers. It is necessary, however, to convert any input signal into a pulse-type waveform before using it to drive a large power load and to convert the signal back into a sinusoidal type signal to recover the original signal. Fig. 19 shows how a sinusoidal signal may be converted into a pulse-type signal using some form of sawtooth or chopping waveform to be applied with the input into a comparator-type op-amp circuit so that a representative pulse-type signal is produced. Although the letter D is used to describe the next type of bias operation after class C, the D could also be considered to stand for "Digital," since that is the nature of the signals provided to the class D amplifier.
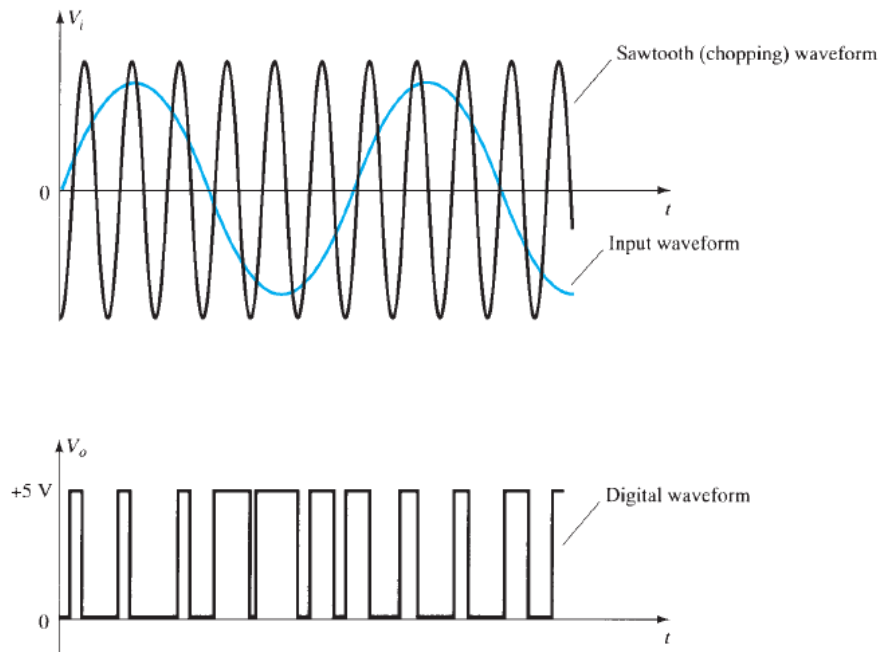
FIG. 19: *Chopping of a sinusoidal waveform to produce a digital waveform.*

Figure 20 shows a block diagram of the unit needed to amplify the class D signal and then convert back into the sinusoidal-type signal using a low-pass filter. Since the amplifier's transistor devices used to provide the output are basically either off or on, they provide current only when they are turned on, with little power loss due to their low "on" voltage. Since most of the power applied to the amplifier is transferred to the load, the efficiency of the circuit is typically very high. Power MOSFET devices have been quite popular as the driver devices for the class D amplifier.
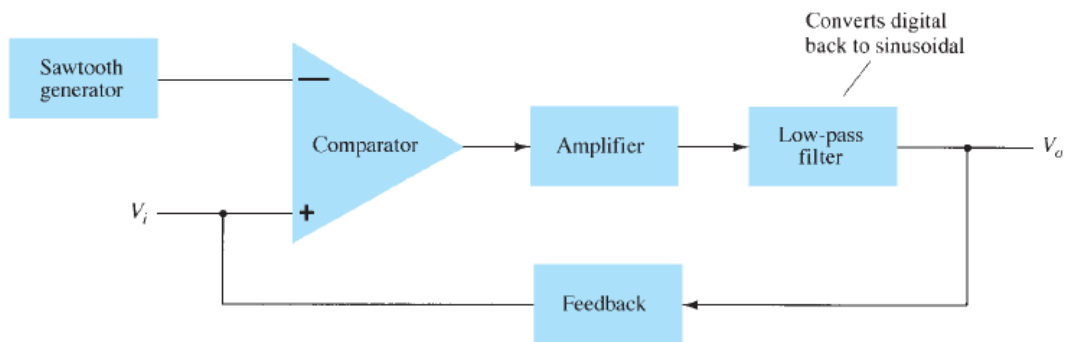
FIG. 20: *Block diagram of class D amplifier.*

Feedback and Oscillator Circuits

FEEDBACK CONCEPTS

Feedback has been mentioned previously in op-amp circuits. Depending on the relative polarity of the signal being feedback into a circuit, one may have negative or positive feedback. **Negative feedback** results in decreased voltage gain, for which a number of circuit features are improved, as summarized below. **Positive feedback** drives a circuit into oscillation as in various types of oscillator circuits.

A typical feedback connection is shown in Fig. 1 . The input signal V_s is applied to a difference block, where it is combined with a feedback signal V_f to produce V_i which is then the input signal to the amplifier (A). A portion of the amplifier output V_o is connected to the feedback block (β), which provides a feedback signal to the difference block.

Feedback amplifier
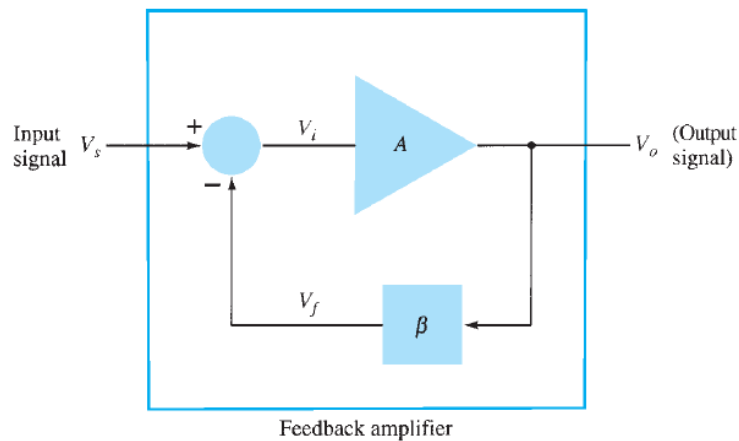
Fig.1

Although negative feedback results in reduced overall voltage gain, a number of advantages are obtained, among them being:

1. Higher input impedance.

2. Better stabilized voltage gain.

3. Improved frequency response.

4. Lower output impedance.

5. Reduced noise.

6. More linear operation.

FEEDBACK CONNECTION TYPES

There are four basic ways of connecting the feedback signal. Both voltage and current can be feedback to the input either in series or parallel. Specifically, there can be:

1. Voltage-series feedback (Fig. 2 a).

2. Voltage-shunt feedback (Fig. 2 b).

3. Current-series feedback (Fig. 2 c).

4. Current-shunt feedback (Fig. 2 d).

In the list above, voltage refers to connecting the output voltage as input to the feedback network; current refers to tapping off some output current through the feedback loop. Series refers to connecting the feedback signal in series with the input signal voltage; shunt refers to connecting the feedback signal in shunt (parallel) with an input current source.
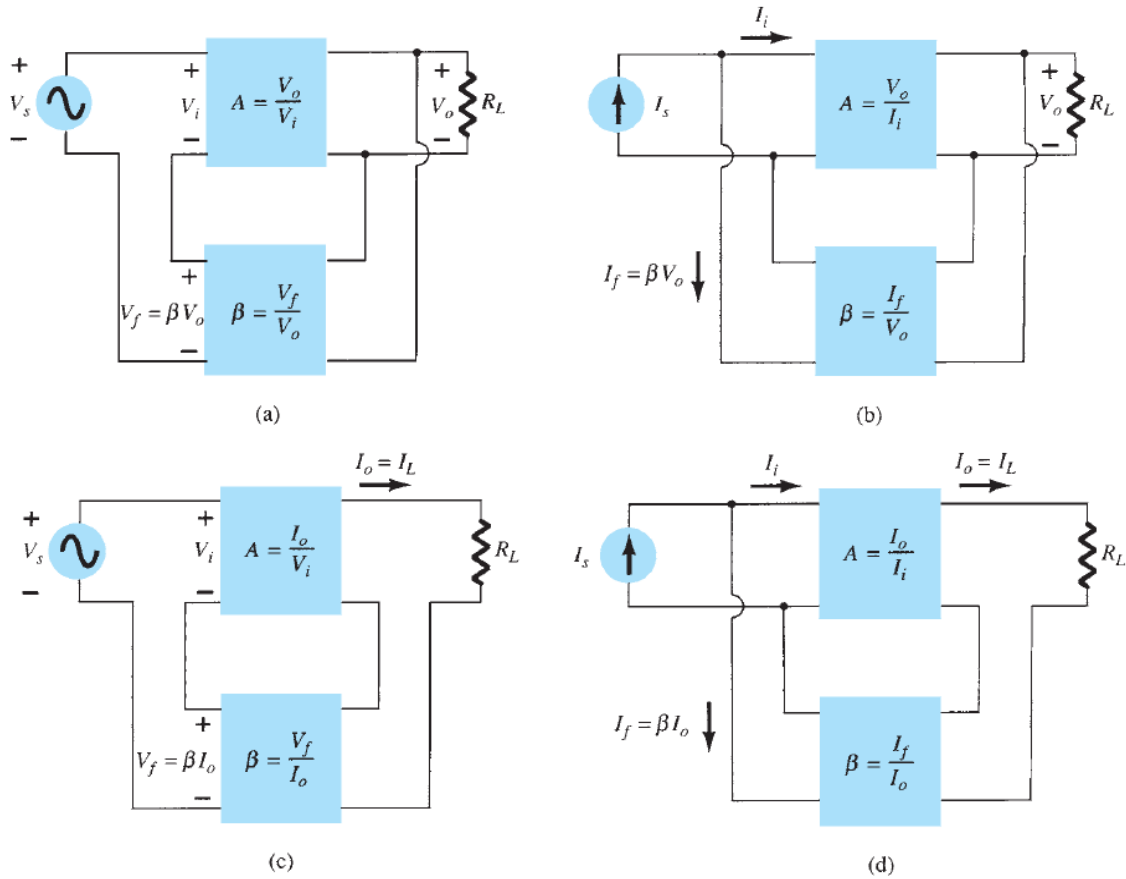
FIG. 2: Feedback amplifier types:

(a) voltage-series feedback, Af = Vo/Vs; (b) voltage-shunt feedback, Af = Vo/Is;

(c) current-series feedback, Af = Io/Vs; (d) current-shunt feedback, Af = Io/Is.

Series feedback connections tend to *increase* the input resistance, whereas shunt feedback connections tend to *decrease* the input resistance. Voltage feedback tends to *decrease* the output impedance, whereas current feedback tends to *increase* the output impedance. Typically, higher input and lower output impedances are desired for most cascade amplifiers. Both of these are provided using the voltage-series feedback connection.

Gain with Feedback

The gain without feedback, A , is that of the amplifier stage. With feedback β, the overall gain of the circuit is reduced by a factor $(1 + \beta A)$. A summary of the gain, feedback factor, and gain with feedback of Fig. 2 is provided for reference in Table 1.

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TABLE 1 *Summary of Gain, Feedback, and Gain with Feedback from Fig. 2*

		Voltage-Series	Voltage-Shunt	Current-Series	Current-Shunt
Gain without feedback	A	$\dfrac{V_o}{V_i}$	$\dfrac{V_o}{I_i}$	$\dfrac{I_o}{V_i}$	$\dfrac{I_o}{I_i}$
Feedback	β	$\dfrac{V_f}{V_o}$	$\dfrac{I_f}{V_o}$	$\dfrac{V_f}{I_o}$	$\dfrac{I_f}{I_o}$
Gain with feedback	A_f	$\dfrac{V_o}{V_s}$	$\dfrac{V_o}{I_s}$	$\dfrac{I_o}{V_s}$	$\dfrac{I_o}{I_s}$

1- Voltage-Series Feedback

Figure 2-a shows the voltage-series feedback connection with a part of the output voltage fed back in series with the input signal, resulting in an overall gain reduction. If there is no feedback ($V_f = 0$), the voltage gain of the amplifier stage is:

$$A = \frac{V_o}{V_s} = \frac{V_o}{V_i} \quad (1)$$

If a feedback signal V_f is connected in series with the input, then

$$V_i = V_s - V_f$$

Since $\quad V_o = AV_i = A(V_s - V_f) = AV_s - AV_f = AV_s - A(\beta V_o)$

then $\quad (1 + \beta A)V_o = AV_s$

so that the overall voltage gain with feedback is

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A} \quad (2)$$

Equation (2) shows that the gain with feedback is the amplifier gain reduced by the factor $(1+\beta A)$. This factor will be seen also to affect input and output impedance among other circuit features.

Input Impedance with Feedback

A more detailed voltage-series feedback connection is shown in Fig. 3 . The input impedance can be determined as follows:

$$I_i = \frac{V_i}{Z_i} = \frac{V_s - V_f}{Z_i} = \frac{V_s - \beta V_o}{Z_i} = \frac{V_s - \beta A V_i}{Z_i}$$

$$I_i Z_i = V_s - \beta A V_i$$

$$V_s = I_i Z_i + \beta A V_i = I_i Z_i + \beta A I_i Z_i$$

$$Z_{if} = \frac{V_s}{I_i} = Z_i + (\beta A)Z_i = Z_i(1 + \beta A) \quad (3)$$

The input impedance with series feedback is seen to be the value of the input impedance without feedback multiplied by the factor $(1+\beta A)$, and applies to both voltage-series (Fig. 2 a) and current-series (Fig. 2 c) configurations.
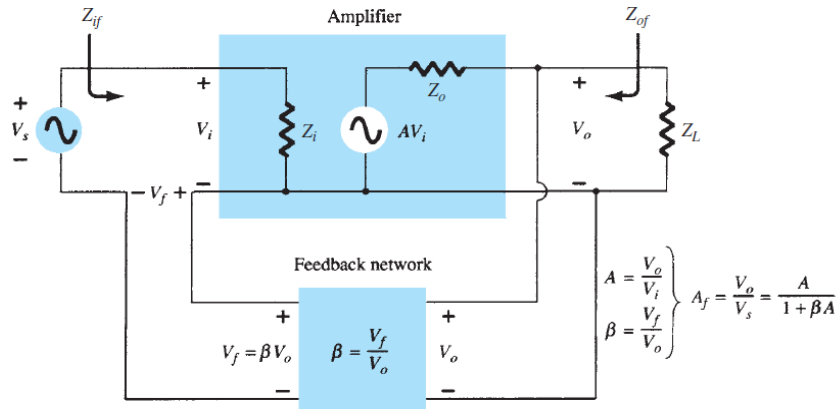
FIG. 3: Voltage-series feedback connection.

Output Impedance with Feedback

The output impedance for the connections of Fig. 2 is dependent on whether voltage or current feedback is used. For voltage feedback, the output impedance is decreased, whereas current feedback increases the output impedance.

For voltage-series feedback, the voltage-series feedback circuit of Fig. 3 provides sufficient circuit detail to determine the output impedance with feedback. The output impedance is determined by applying a voltage V , resulting in a current I , with **Vs** shorted out (Vs = 0). The voltage V is then

$$V = IZ_o + AV_i$$

For $V_s = 0$, $V_i = -V_f$

so that $V = IZ_o - AV_f = IZ_o - A(\beta V)$

Rewriting the equation as

$$V + \beta AV = IZ_o$$

allows solving for the output impedance with feedback:

$$Z_{of} = \frac{V}{I} = \frac{Z_o}{1 + \beta A} \qquad (4)$$

2- Voltage-Shunt Feedback

The gain with feedback for the network of Fig. 2-b is

$$A_f = \frac{V_o}{I_s} = \frac{A I_i}{I_i + I_f} = \frac{A I_i}{I_i + \beta V_o} = \frac{A I_i}{I_i + \beta A I_i}$$

$$A_f = \frac{A}{1 + \beta A} \qquad (5)$$

4

A more detailed voltage-shunt feedback connection is shown in Fig. 4. The input impedance can be determined to be

$$Z_{if} = \frac{V_i}{I_s} = \frac{V_i}{I_i + I_f} = \frac{V_i}{I_i + \beta V_o}$$

$$= \frac{V_i/I_i}{I_i/I_i + \beta V_o/I_i}$$

$$Z_{if} = \frac{Z_i}{1 + \beta A} \qquad (6)$$

This reduced input impedance applies to the voltage-series connection of Fig. 2-a and the voltage-shunt connection of Fig. 2-b.
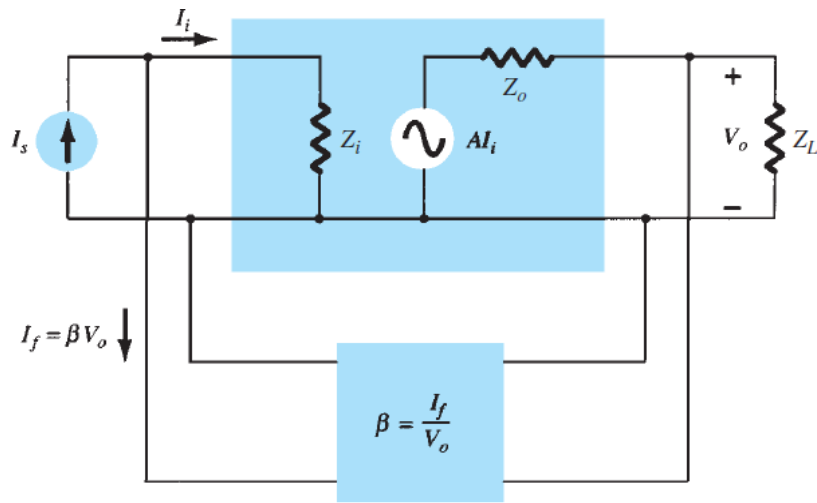
FIG. 4: Voltage-shunt feedback connection.

The output impedance with current-series feedback can be determined by applying a signal V to the output with Vs shorted out, resulting in a current I , the ratio of V to I being the output impedance. Figure 5 shows a more detailed connection with current-series feedback. For the output part of a current-series feedback connection shown in Fig. 5 , the resulting output impedance is determined as follows.

With V s =0,

$$V_i = V_f$$

$$I = \frac{V}{Z_o} - AV_i = \frac{V}{Z_o} - AV_f = \frac{V}{Z_o} - A\beta I$$

$$Z_o(1 + \beta A)I = V$$

$$Z_{of} = \frac{V}{I} = Z_o(1 + \beta A) \qquad (7)$$
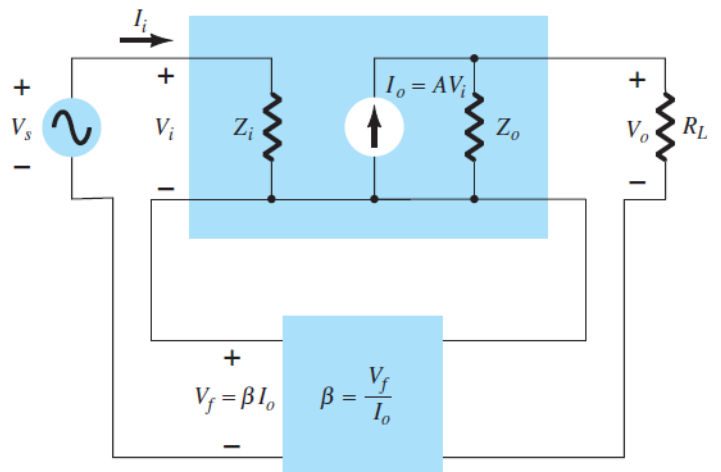
Fig.5

A summary of the effect of feedback on input and output impedance is provided in Table 2.

TABLE 2 *Effect of Feedback Connection on Input and Output Impedance*

Voltage-Series	Current-Series	Voltage-Shunt	Current-Shunt
$Z_{if} \ Z_i(1 + \beta A)$	$Z_i(1 + \beta A)$	$\dfrac{Z_i}{1 + \beta A}$	$\dfrac{Z_i}{1 + \beta A}$
(increased)	(increased)	(decreased)	(decreased)
$Z_{of} \ \dfrac{Z_o}{1 + \beta A}$	$Z_o(1 + \beta A)$	$\dfrac{Z_o}{1 + \beta A}$	$Z_o(1 + \beta A)$
(decreased)	(increased)	(decreased)	(increased)

EXAMPLE 1   Determine the voltage gain, input, and output impedance with feedback for voltage-series feedback having $A = -100, R_i = 10\text{ k}\Omega$, and $R_o = 20\text{ k}\Omega$ for feedback of (a) $\beta = -0.1$ and (b) $\beta = -0.5$.

Solution:

a. $A_f = \dfrac{A}{1 + \beta A} = \dfrac{-100}{1 + (-0.1)(-100)} = \dfrac{-100}{11} = -9.09$

$Z_{if} = Z_i(1 + \beta A) = 10\text{ k}\Omega \ (11) = 110\text{ k}\Omega$

$Z_{of} = \dfrac{Z_o}{1 + \beta A} = \dfrac{20 \times 10^3}{11} = 1.82\text{ k}\Omega$

b. $A_f = \dfrac{A}{1 + \beta A} = \dfrac{-100}{1 + (-0.5)(-100)} = \dfrac{-100}{51} = -1.96$

$Z_{if} = Z_i(1 + \beta A) = 10\text{ k}\Omega \ (51) = 510\text{ k}\Omega$

$Z_{of} = \dfrac{Z_o}{1 + \beta A} = \dfrac{20 \times 10^3}{51} = 392.16\ \Omega$

Example 1 demonstrates the trade-off of gain for desired input and output resistance. Reducing the gain by a factor of 11 (from 100 to 9.09) is complemented by a reduced output resistance and increased input resistance by the same factor of 11. Reducing the gain by a factor of 51 provides a gain of only 2 but with input resistance increased by the factor of 51 (to over 500 kΩ) and output resistance reduced from 20 kΩ to under 400 Ω. Feedback offers the designer the choice of trading away some of the available amplifier gain for other desired circuit features.

PRACTICAL FEEDBACK CIRCUITS

Examples of practical feedback circuits will provide a means of demonstrating the effect feedback has on the various connection types. This section provides only a basic introduction to this topic.

Voltage-Series Feedback

Figure 6 shows a voltage-series feedback connection using an op-amp. The gain of the op-amp, A , without feedback, is reduced by the feedback factor

$$\beta = \dfrac{R_2}{R_1 + R_2}$$

6
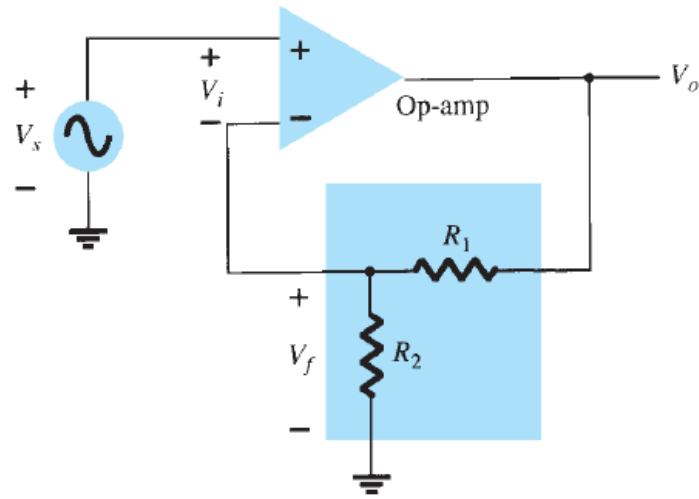
FIG. 6: *Voltage-series feedback in an op-amp connection.*

EXAMPLE 2 Calculate the amplifier gain of the circuit of Fig. 5 for op-amp gain $A = 100{,}000$ and resistances $R_1 = 1.8\,\text{k}\Omega$ and $R_2 = 200\,\Omega$.

Solution:

$$\beta = \frac{R_2}{R_1 + R_2} = \frac{200\,\Omega}{200\,\Omega + 1.8\,\text{k}\Omega} = 0.1$$

$$A_f = \frac{A}{1 + \beta A} = \frac{100{,}000}{1 + (0.1)(100{,}000)}$$

$$= \frac{100{,}000}{10{,}001} = 9.999$$

Note that since $\beta A \gg 1$,

$$A_f \cong \frac{1}{\beta} = \frac{1}{0.1} = 10$$

Voltage-Shunt Feedback

The constant-gain op-amp circuit of Fig. 7-a provides voltage-shunt feedback. Referring to Fig.7- b and Table 1 and the op-amp ideal characteristics $Ii = 0$, $Vi = 0$, and voltage gain of infinity, we have

$$A = \frac{V_o}{I_i} = \infty$$

$$\beta = \frac{I_f}{V_o} = \frac{-1}{R_o}$$

The gain with feedback is then

$$A_f = \frac{V_o}{I_s} = \frac{V_o}{I_i} = \frac{A}{1 + \beta A} = \frac{1}{\beta} = -R_o$$

This is a transfer resistance gain. The more usual gain is the voltage gain with feedback,

$$A_{vf} = \frac{V_o}{I_s} \frac{I_s}{V_1} = (-R_o)\frac{1}{R_1} = \frac{-R_o}{R_1}$$
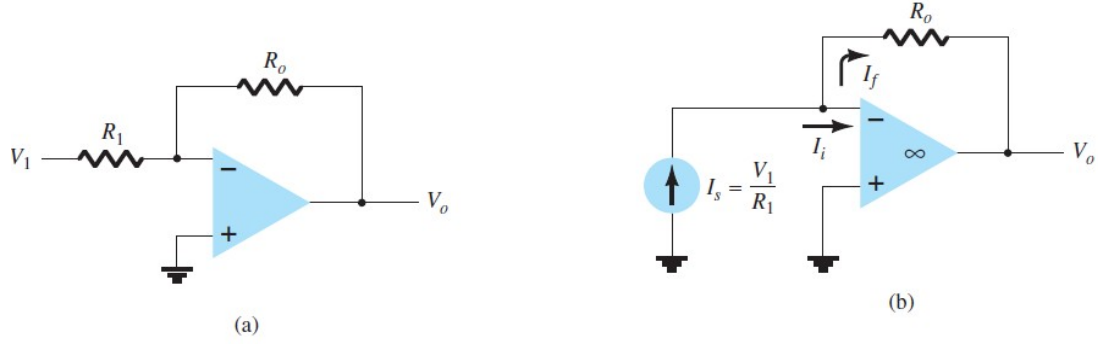
FIG. 6: *Voltage-shunt negative feedback amplifier: (a) constant-gain circuit; (b) equivalent circuit.*

SUMMARY of Equations

Voltage-series feedback:

$$A_f = \frac{V_o}{V_s} = \frac{A}{1 + \beta A}, \qquad Z_{if} = \frac{V_s}{I_i} = Z_i + (\beta A)Z_i = Z_i(1 + \beta A),$$

$$Z_{of} = \frac{V}{I} = \frac{Z_o}{(1 + \beta A)}$$

Voltage-shunt feedback:

$$A_f = \frac{A}{1 + \beta A}, \qquad Z_{if} = \frac{Z_i}{(1 + \beta A)}$$

Current-series feedback:

$$Z_{if} = \frac{V}{I} = Z_i(1 + \beta A), \qquad Z_{of} = \frac{V}{I} = Z_o(1 + \beta A)$$

Current shunt feedback:

$$Z_{if} = \frac{Z_i}{(1 + \beta A)}, \qquad Z_{of} = \frac{V}{I} = Z_o(1 + \beta A)$$

8

OP-AMP and its applications

Introduction

- The operational amplifier (Op-Amp) concept was introduced by Tellegen in 1954 under the name of "ideal amplifier". The first Op-Amps with discrete transistors appeared in production in 1956. One of the first analog ICs was an Op-Amp developed by R. Widlar in 1964. The operational amplifier is still the integrated circuit with highest production volume.

- OP-AMP is a very high-gain directly-coupled negative-feedback amplifier which can amplify signals having frequency ranging from **0 Hz to 1 MHz.**

- OP-AMP is so named because it was originally designed to perform mathematical operations like summation, subtraction, multiplication, differentiation integration …etc. Present day usage is much wider in scope but the popular name OP-AMP continues.

nd in analog computers applications.

- Typical applications of OP-AMP are scale changing, analog computer operations, in instrumentation and control systems and a great variety of phase-shift and oscillator circuits.

- Example of OP-AMPs [LM 108, LM 208, 741,….]

OP-AMP Circuit and Symbol

Standard triangular symbol of an OP-AMP is shown in Fig.1. All OP-AMPs have a minimum of five terminals:

1. inverting input terminal (labeled with a minus sign),

2. non-inverting input terminal (labeled with a plus sign),

3. output terminal,

4. positive bias supply terminal,

5. negative bias supply terminal.
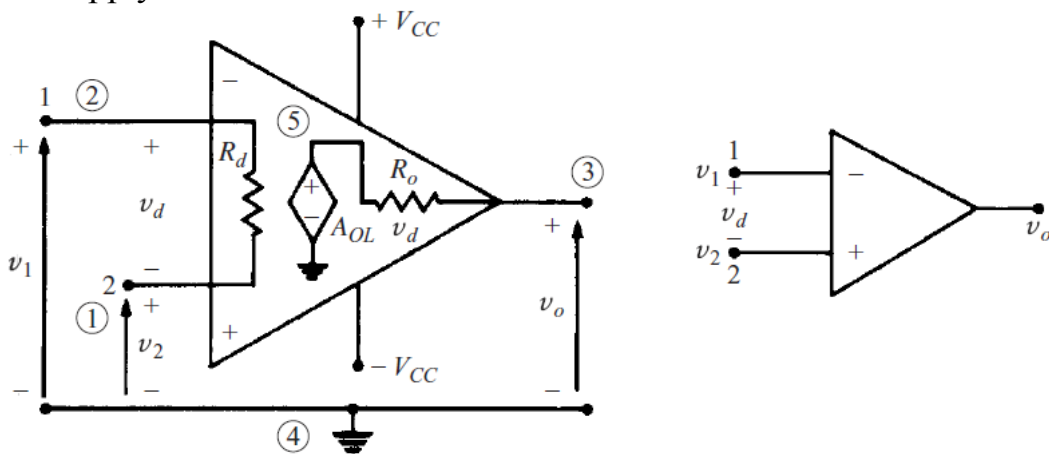
(a) Complete representation   (b) Simplified representation

Fig. 1: Operational amplifier

- When an OP-AMP is operated without connecting any resistor or capacitor from its output to any one of its inputs (*i.e.*, without feedback), it is said to be in the **open-loop condition**. The specifications of OP-AMP under such condition are called open-loop specifications and exhibiting the open-loop voltage gain (A_{OL}).

- An op amp amplifies the difference between two input signals v_1 & v_2; i.e amplifies (v_d), where ($v_d = v_1 - v_2$)

$$v_o = A_{OL} * v_d \quad (A_{OL} \text{ for actual op amp is extremely high } i.e., \text{ about } 10^6)$$

However, if ($v_d = 1$ V), it does not mean that will be amplified to 10^6 V at the output.

Actually, the maximum value of v is limited by the basis supply voltage and is called its **saturation voltage**. This voltage is approximately 2V smaller than the power-supply voltage (V_{CC}). In other words, the amplifier is linear over the range

$$-(V_{CC} - 2) < v_o < V_{CC} - 2 \text{ , typically } \pm 15 \text{ V.}$$

Example1: An op amp has saturation voltage Vsat =10 V, an open-loop voltage gain of -10 [5], and input resistance of 100k. Find (a) the value of v that will just drive the amplifier to saturation and (b) the op amp input current at the starting of saturation.

Solution:

(a) $v_d = \dfrac{\pm V_{osat}}{A_{OL}} = \dfrac{\pm 10}{-10^5} = \pm 0.1 \text{ mV}$

(b) $i_{in} = \dfrac{v_d}{R_d} = \dfrac{\pm 0.1 \times 10^{-3}}{100 \times 10^3} = \pm 1 \text{ nA}$

Ideal Operational Amplifier

An ideal *OP-AMP* has the following characteristics :

1. its open-loop gain A_{OL} is *infinite* i.e., $Av = -\infty$

2. its input resistance Ri (measured between inverting and non-inverting terminals) is *infinite* i.e., $Ri = \infty \, \Omega$. This means that the input current $i = 0$.

3. its output resistance R_0 (seen looking back into output terminals) is *zero* i.e., $R_0 = 0 \, \Omega$. This means that v_0 is not dependent on the load resistance connected across the output.

4. it has *infinite bandwith* i.e., it has flat frequency response from dc to infinity.

Virtual Ground and Summing Point

Fig. 2 shows an *OP-AMP* which *employs **negative feedback*** with the help of resistor R_f which feeds a portion of the output to the input. The concept of **virtual** ground arises from the fact that input voltage vi at the inverting terminal of the *OP-AMP* is forced to a small value (assumed zero). Hence, point A is essentially at ground voltage and is referred to as *virtual ground*. Obviously, *it is not the actual ground.*

When v1 is applied, point A attains some positive potential and at the same time v_0 is brought into existence. Due to negative feedback, some fraction of the output voltage is fed back to point A antiphase with the voltage already existing there (due to v1). The algebraic sum of the two voltages is almost zero so that $vi \cong 0$. Obviously, vi will become exactly zero when **negative feedback voltage at A is exactly equal to the positive voltage produced by v1 at A.**
Another point worth considering is that there exists a virtual short between the two terminals of the *OP-AMP* because $vi = 0$. It is virtual because no current flows (remember $i = 0$) despite the existence of this short.
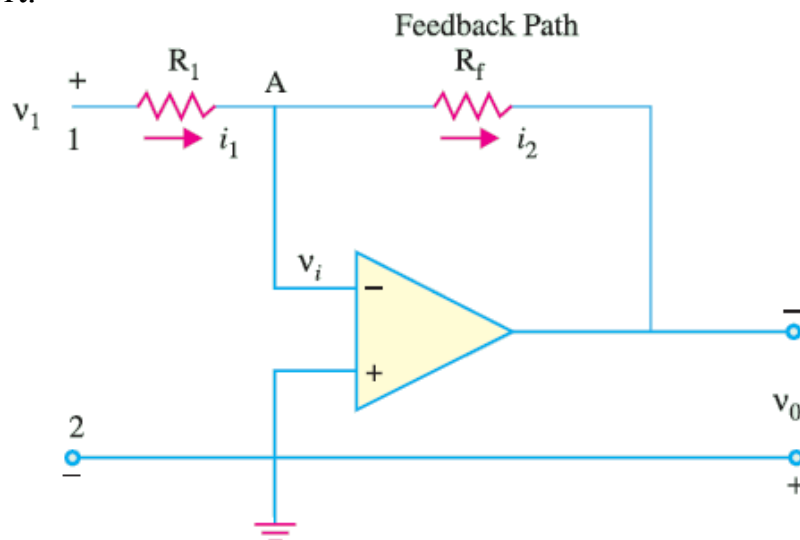
Fig. 2

OP-AMP Applications
1- Inverting Amplifier
The inverting amplifier of Fig. 3 has its noninverting input connected to ground. A signal (vin) is applied through input resistor R1, and negative current feedback is implemented through feedback resistor R_f. Output voltage (v_o) has polarity opposite that of input.
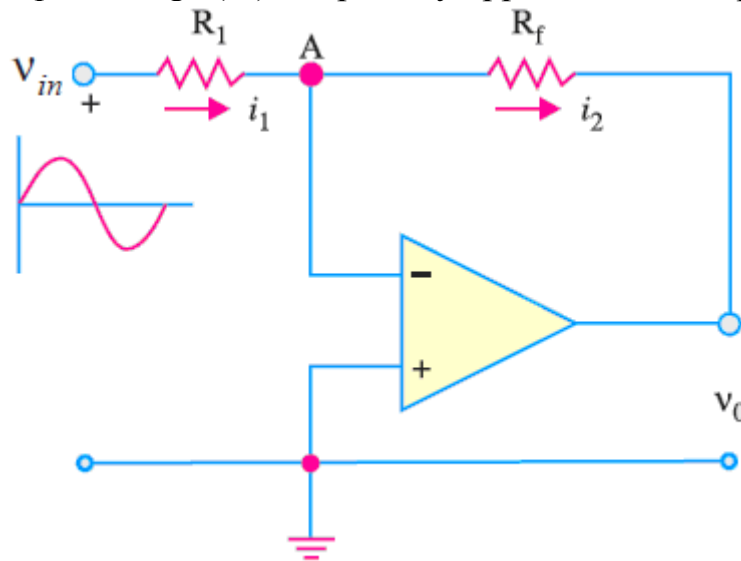
Fig. 3

The gain of the inverting amplifier can be driven as follow:
Since point A is at ground potential ($V_A=0$) and $i_{in}=0$,

$$i1=i2 \implies i_1 = \frac{V_{in}-V_A}{R_1} \quad \text{and} \quad i_2 = \frac{V_A - V_0}{R_f}$$

$$\frac{V_{in}-0}{R_1} = \frac{0-V_0}{R_f} \implies \frac{V_0}{R_f} = -\frac{V_{in}}{R_1} \quad \text{or} \quad \frac{V_0}{V_{in}} = -\frac{R_f}{R_1}$$

$$A_v = -\frac{R_f}{R_1} \quad \text{Also, } V_0 = -A_v V_{in}$$

It is seen from above, that closed-loop gain of the inverting amplifier depends on the ratio of the two external resistors $R1$ and Rf and is independent of the amplifier parameters.

2- Noninverting Amplifier
The noninverting amplifier of Fig. 4 is realized by grounding R1 of Fig. 3 and applying the input signal at the noninverting. Here, polarity of v0 is the same as that vin.
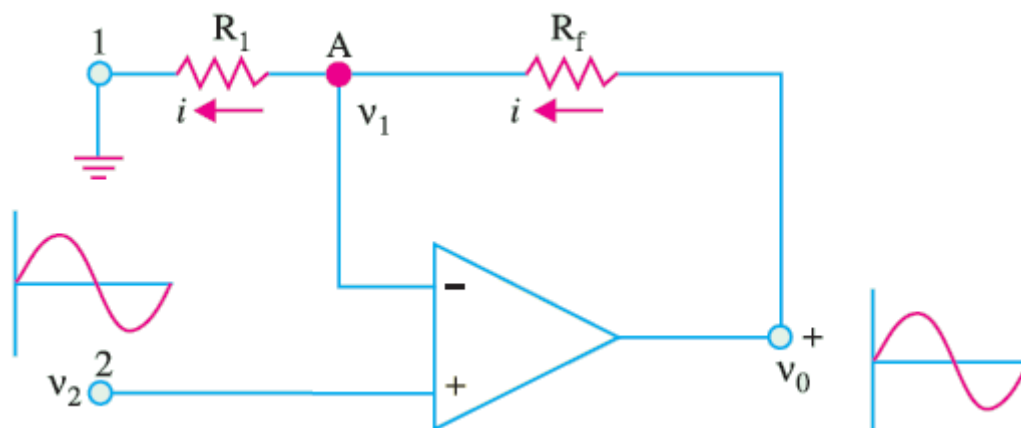
Fig. 4

The gain of the noninverting amplifier can be driven as follow:

Because of virtual short between the two *OP-AMP* terminals, voltage across R1 is the input voltage vin. Also, v0 is applied across the series combination of *R1* and *Rf*.

$$\therefore V_{in} = iR_1 \quad, V_0 = i(R_1 + R_f)$$

$$A_v = \frac{V_0}{V_{in}} = \frac{i(R_1 + R_f)}{iR_1} \quad \text{or} \quad A_v = \frac{R_1 + R_f}{R_1} = \left(1 + \frac{R_f}{R_1}\right)$$

3- Voltage Follower

It provides a gain of unity without any phase reversal. This circuit (Fig. 5) is useful as a buffer or isolation amplifier because it allows, input voltage vin to be transferred as output voltage v0 while at the same time preventing load resistance *RL* from loading down the input source. It is due to the fact that its $R_i = \infty$ and $R_0 = 0$.

$$(V_{in} = V_0)$$
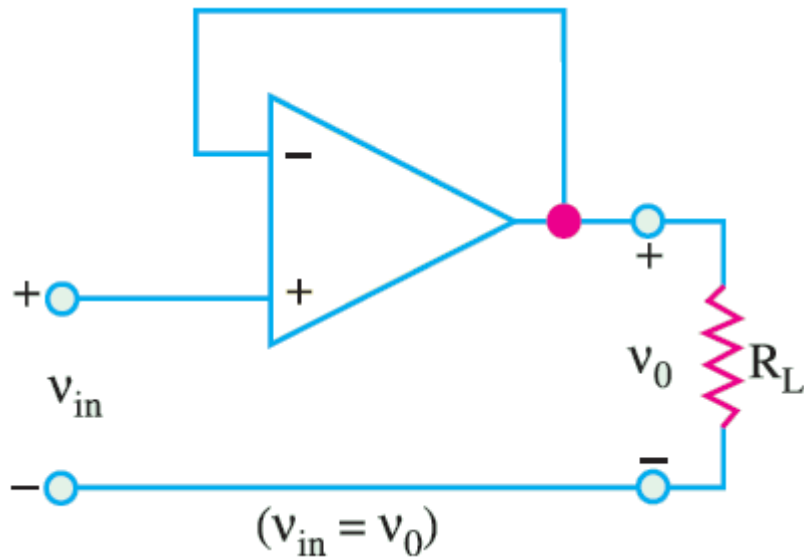
Fig. 5

4- Adder or Summer Amplifier

The adder circuit provides an output voltage proportional to or equal to the algebraic sum of two or more input voltages each multiplied by a constant gain factor. It is basically similar to a Fig. 3 except that it has more than one input. Fig. 6 shows a three-input inverting adder circuit. As seen, *the **output voltage is phase-inverted.***
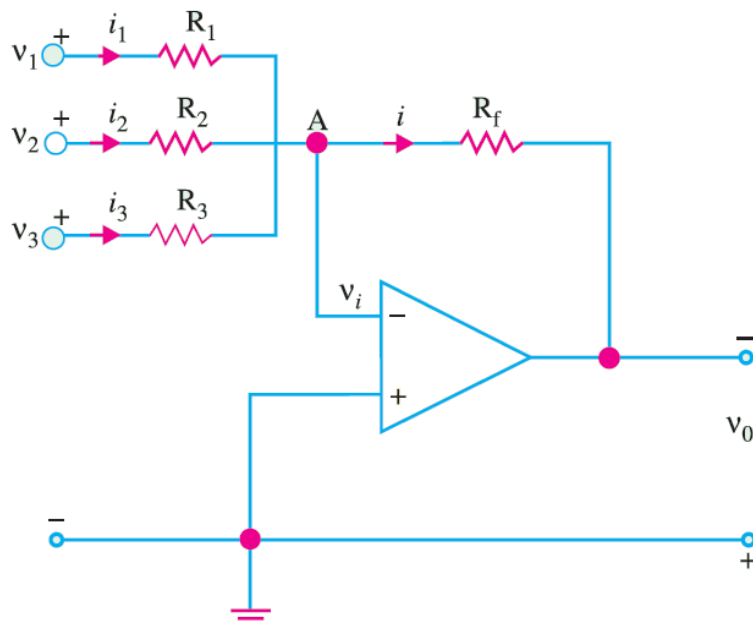
Fig. 6

Calculations

As before, we will treat point A as virtual ground

$$i_1 = \frac{v_1}{R_1} \quad , \quad i_2 = \frac{v_2}{R_2} \quad , \quad i_3 = \frac{v_3}{R_3} \quad \text{and} \quad i = -\frac{v_0}{R_f}$$

Applying *KCI* to point A, we have

$$i_1 + i_2 + i_3 + (-i) = 0$$

or

$$\frac{v_1}{R_1} + \frac{v_2}{R_2} + \frac{v_3}{R_3} - \left(\frac{-v_0}{R_f} \right) = 0$$

$$\therefore \quad v_0 = -\left(\frac{R_f}{R_1} v_1 + \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3 \right)$$

If $R_1 = R_2 = R_3 = R$, then

$$v_0 = -\frac{R_f}{R} (v_1 + v_2 + v_3)$$

If $R_f = R$, then ouput exactly equals the sum of inputs.

5- Subtractor

The function of a subtractor is to provide an output proportional to the difference of two input signals. As shown in Fig. 7. The inputs are applying at the inverting and noninverting terminals.
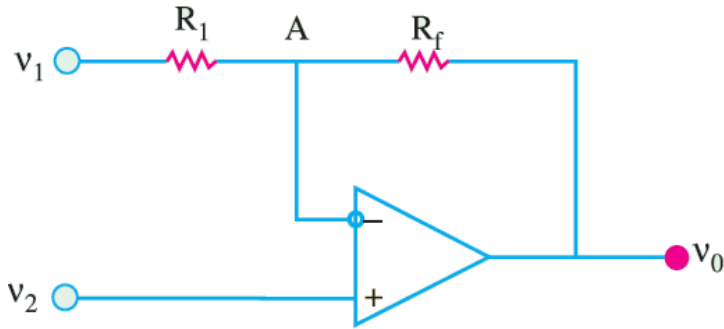
Fig. 7

Calculations

According to Superposition theorem;

$v0 = v0' + v0''$

where $v0'$ is the output produced by v1 and $v0''$ is that produced by v2.

Now $v_0' = -\dfrac{R_f}{R_1} \cdot v_1$ (see inverting amplifier equation)

$v_0'' = \left(1 + \dfrac{R_f}{R_1}\right) v_2$ (see noninverting amplifier equation)

If $Rf \gg R1$ and $Rf/R1 \gg 1$, hence

$v_0 \cong \dfrac{R_f}{R_1}(v_2 - v_1)$

Further, If $Rf = R1$, then

$v0 = (v2 - v1) =$ difference of the two input voltages

Example: Find the output voltages of an OP-AMP inverting adder for the following sets of input voltages and resistors. In all cases, Rf = 1 MΩ.
v1 = −3 V, v2 = + 3V, v3 = + 2V; R1 = 250 KΩ, R2 = 500 KΩ, R3 = 1 M Ω (ans. Vo=4v)

Example: In the subtractor circuit, R1 = 5 K, Rf = 10 K, v1 = 4 V and v2 = 5V. Find the value of output voltage.

Solution:

$v_0 = \left(1 + \dfrac{R_f}{R_1}\right)v_1 - \dfrac{R_f}{R_1}v_2 = \left(1 + \dfrac{10}{5}\right)4 - \dfrac{10}{5} \times 5 = + \mathbf{2V}$

Example: Design an OP-AMP circuit that will produce an output equal to − (4 v1 + v2 +0·1v3). Write an expression for the output and sketch its output waveform when v1 = 2 sin ωt, v2 =+5V dc and v3 = −100 Vdc.

Solution:

$$v_0 = -\left[\dfrac{R_f}{R_1}v_1 + \dfrac{R_f}{R_2}v_2 + \dfrac{R_f}{R_3}v_3\right] \quad ...(1)$$

$$v_0 = -(4\,v_1 + v_2 + 0\cdot1\,v_3) \quad ...(2)$$

Comparing equations **(1)** and **(2)**, we find,

$$\frac{R_f}{R_1} = 4, \quad \frac{R_f}{R_2} = 1, \quad \frac{R_f}{R_3} = 0\cdot1$$

Therefore if we assume $R_f = 100\ K$, then $R1 = 25\ K$, $R2 = 100\ K$ and $R3 = 10\ K$. With there values of $R1$, $R2$ and $R3$, the *OP-AMP* circuit is as shown in Fig. 8 *(a)*.
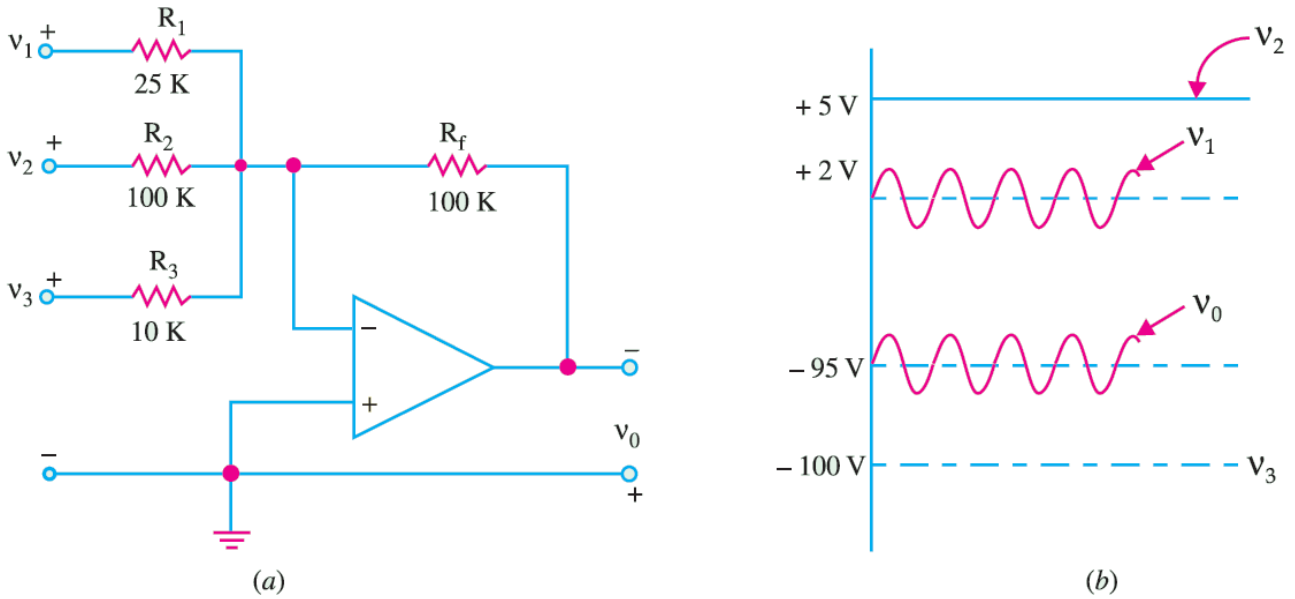
Fig. 8

With the given values of $v1 = 2 \sin \omega t$, $v2 = + 5V$, $v3 = -100$ V dc, the output voltage, $v0 = 2\sin \omega t + 5 - 100 = 2 \sin \omega t - 95$ V. The waveform of the output voltage is sketched as shown in Fig.8 *(b)*.

6- Integrator

The function of an integrator is to provide an output voltage which is proportional to the integral of the input voltage. A simple example of integration is shown in Fig. 9, where input is dc level and its integral is *a linearly-increasing ramp output.* The actual integration circuit is similar to the inverting circuit except that **the feedback component is a capacitor C instead of a resistor Rf.**
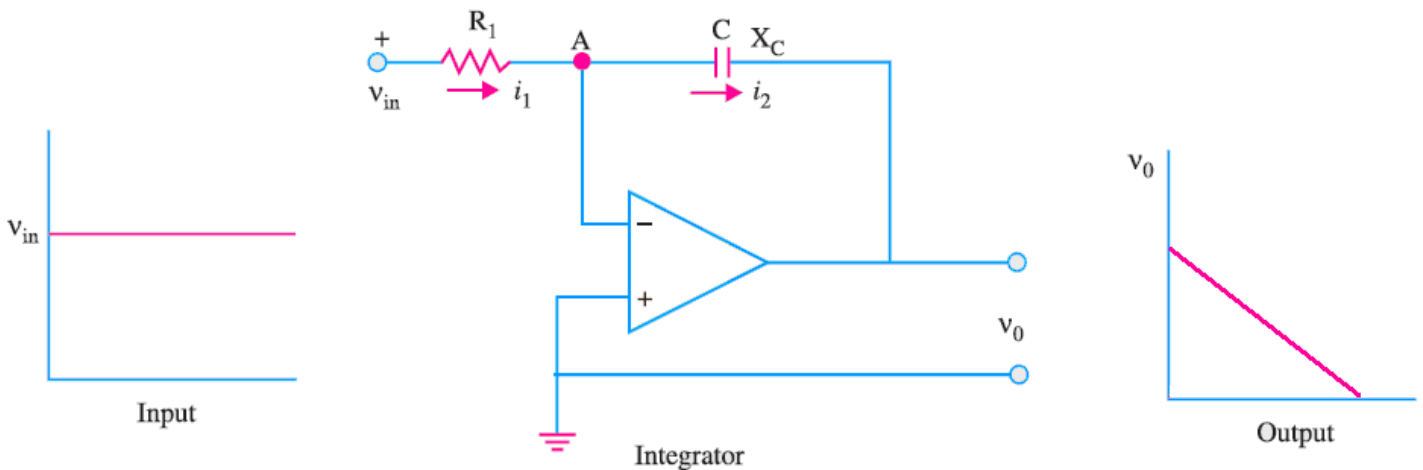
Fig. 9

Calculations

As before, If the op amp is ideal, point A will be treated as virtual ground, and v_{in} appears across R_1. Thus

$$i_1 = \frac{v_{in}}{R_1}$$

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$$i_2 = i_c = c\frac{dv_c}{dt} = -c\frac{dv_o}{dt} \quad \text{(since } v_c = -v_o\text{)}$$

But, with negligible current into the op amp, the current through R1 = current flow through C. Then

$$\frac{v_{in}}{R_1} = -c\frac{dv_o}{dt} \quad \Rightarrow \quad dv_0 = -\frac{1}{R_1 c}v_{in}dt \quad \Rightarrow \quad v_o = -\frac{1}{R_1 c}\int v_{in}dt$$

It is seen from above that output (left-hand side) is an integral of the input, with an inversion and a scale factor of $1/CR_1$. This ability to integrate a given signal enables an analog computer solve differential equations and to set up a wide variety of electrical circuit analogs of physical system operation.

Note: we can integrate more than one input as shown below in Fig. 10. With multiple inputs, the output is given by

$$v_0(t) = -\left[K_1\int v_1(t)\,dt + K_2\int v_2(t)\,dt + k_3\int v_3(t)\,dt\right]$$

where $\quad K_1 = \dfrac{1}{CR_1}, K_2 = \dfrac{1}{CR_2} \quad$ and $\quad K_3 = \dfrac{1}{CR_3}$
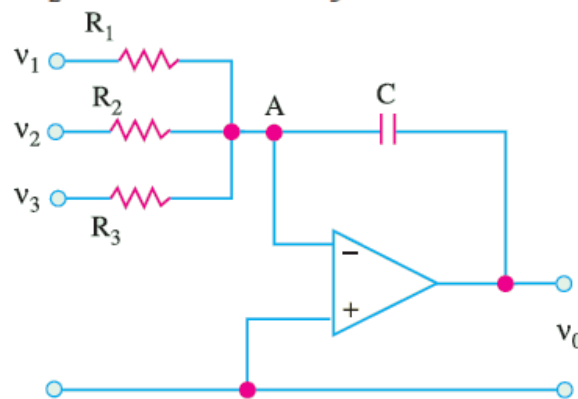
Fig. 10

Example: A 5mV, 1-kHz sinusoidal signal is applied to the input of an OP-AMP integrator, for which R = 100 K and C = 1 μF. Find the output voltage.

Solution:

$$-\frac{1}{CR} = \frac{1}{10^5 \times 10^{-6}} = -10$$

The equation for the sinusoidal voltage is

$$v_1 = 5\sin 2\pi ft = 5\sin 2000\,\pi t$$

Obviously, it has been assumed that at $t = 0$, $v_1 = 0$

$$v_0(t) = -10\int_0^t 5\sin 2000\,\pi t = -50\left.\frac{-\cos 2000\,\pi t}{2000}\right|_0^t$$

$$= -\frac{1}{40\,\pi}(\cos 2000\,\pi t - 1)$$

7- Differentiator

Its function is to provide an output voltage which is **proportional to the rate of the change of the input voltage.** It is an inverse mathematical operation to that of an integrator. As shown in

Fig. 11, when we feed a differentiator with linearly-increasing ramp input, we get a constant dc output.

Differentiator circuit can be obtained by interchanging the resistor and capacitor of the integrator circuit.
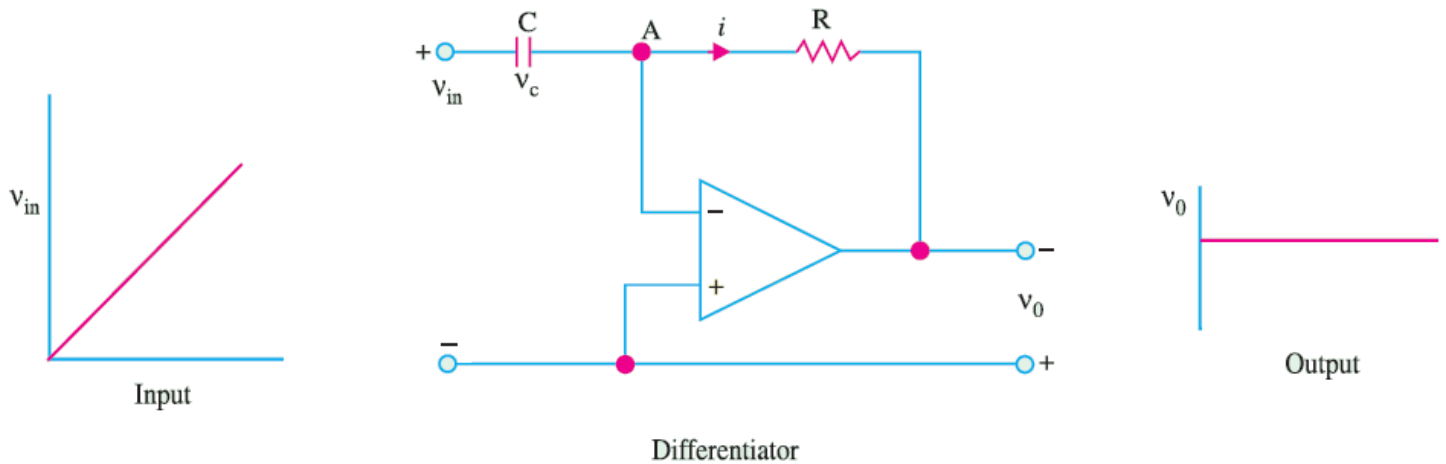
Differentiator

Fig. 11

Calculation:

The expression for the output signal of the inverting differentiator amplifier assuming the op amp is ideal can be derived as follows:

Taking point A as virtual ground, consequently, v_{in} appears across capacitor ($v_{in}=v_c$)

$$i = c\frac{dv_c}{dt} = -c\frac{dv_{in}}{dt}$$

$$v_o = -v_R = -iR = -c\frac{dv_{in}}{dt}R = -cR\frac{dv_{in}}{dt}$$

As seen, output voltage is proportional to the derivate of the input voltage, the constant of proportionality (*i.e.,* scale factor) being ($-RC$).

Example: The input to the differentiator circuit is a sinusoidal voltage of peak value of 5 mV and frequency 1 kHz. Find out the output if R = 1000 K and C = 1 µF.

Solution

The equation of the input voltage is $v1 = 5\sin 2\pi \times 1000\,t = 5\sin 2000\,\pi t$ mV

scale factor $= CR = 10^{-6} \times 10^5 = 0.1$

$$v_0 = 0.1\frac{d}{dt}(5\sin 2000\,\pi t) = (0.5 \times 2000\,\pi)\cos$$

dt (5 sin 2000 πt) = (0·5 × 2000 π) cos 2000 πt = 1000 π cos 2000 πt mV

As seen, output is a cosinusoidal voltage of frequency 1 kHz and peak value 1000 π mV.

8- Comparator

It is a circuit which compares two signals or voltage levels. The circuit is the simple because it needs no additional external components shown in Fig. 12. If v1 and v2 are equal, then v0 should ideally be zero.
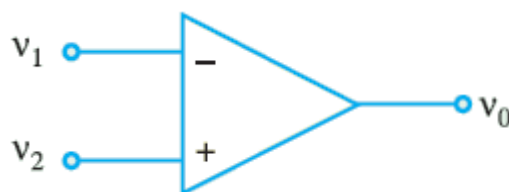
Fig. 12

Output of the comparator can be summarized as follows

If $V_1 > V_2$ then $V_o = -V_{cc}$ (Vsat)

If $V_1 < V_2$ then $V_o = V_{cc}$ (Vsat)

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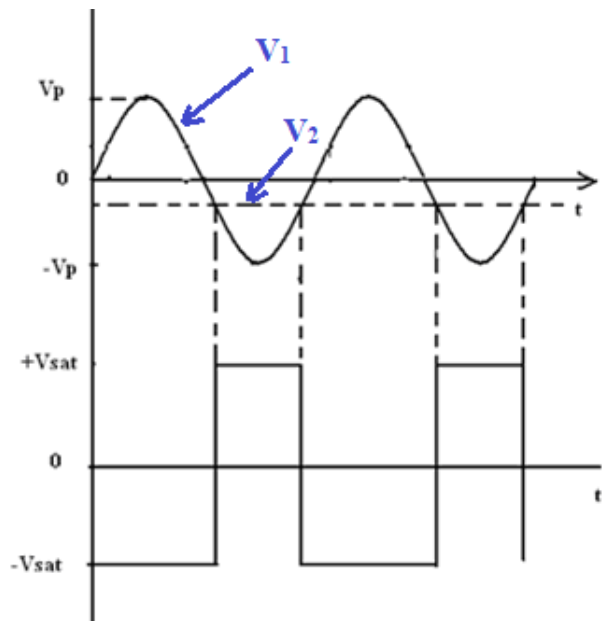
Fig. 13

Application of comparator
1- Zero Crossing Detector
Comparator can be used as a zero crossing detector. A typical circuit for such a detector is shown below:
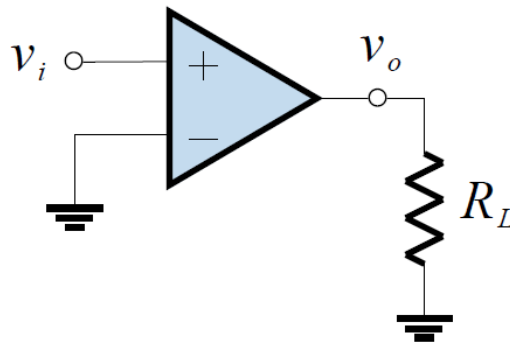
Fig. 14

During the positive half-cycle, the input voltage is positive, hence the output voltage is $+V\text{sat}$. During the negative half-cycle, the input voltage is negative, hence the output voltage is $-V\text{sat}$. Thus the output voltage switches between +Vsat and -Vsat whenever the input signal crosses the zero level.
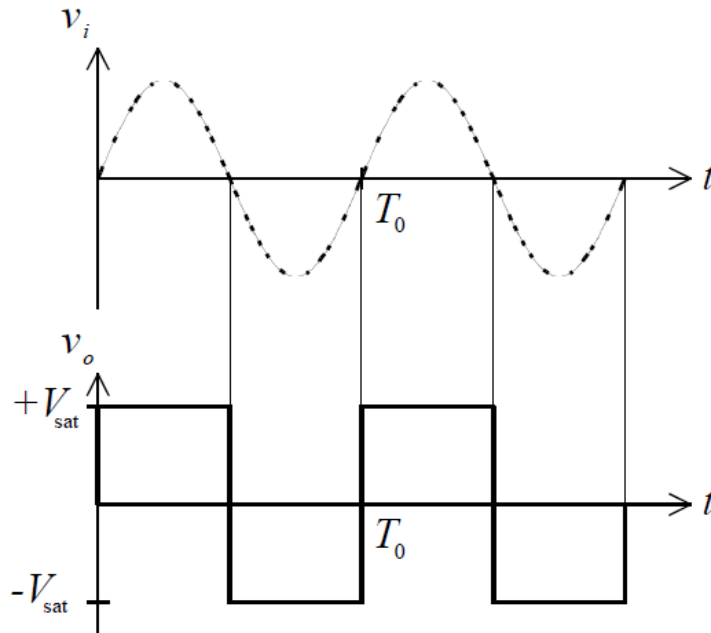
Fig. 15

Looking at the waveform shown above, we realize that a zero crossing detector can be used as a sine- to square-wave converter. This is an impractical circuit, since any noise on the input waveform near the zero crossings will cause multiple level transitions in the output signal (cause a comparator to erratically switch output states). In order to make the comparator less sensitive to noise, a comparator with positive feedback, called **hysteresis**, can be used. This comparator is called Schmitt trigger.

2- Output Bounding (or Voltage limiter)
In some applications, it is necessary to limit the output voltage levels of a comparator to a value less than the saturation voltage. A single zener diode can be used, as shown in Fig. 16, to limit the output voltage to the zener voltage in one direction and to the forward diode voltage drop in the other. This process of limiting the output range is called **bounding**.
The operation is as follows. Since the anode of the zener is connected to the inverting input, it is at virtual ground Therefore, when the output voltage reaches a positive value equal to the zener voltage, it limits at that value, as illustrated in Figure 17(a). When the output switches negative, the zener acts as a regular diode and becomes forward-biased at 0.7 V, limiting the negative output voltage to this value, as shown in part (b). Turning the zener around limits the output voltage in the opposite direction.

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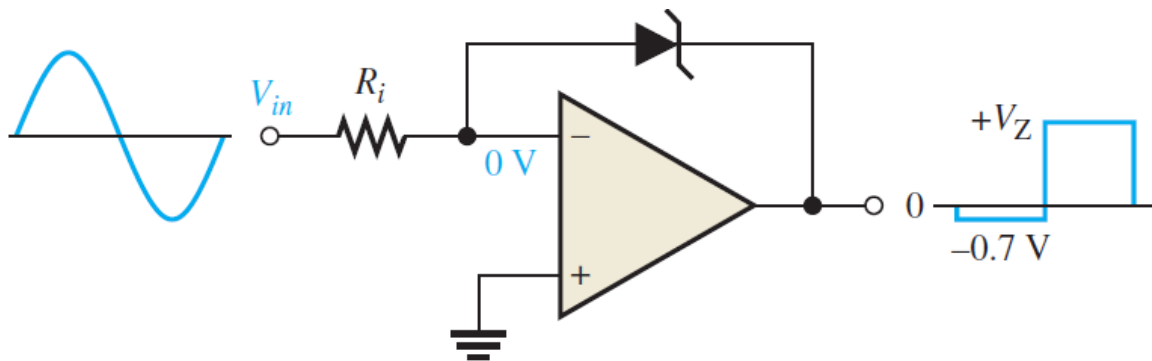
Fig. 17-(a) Bounded at a positive value
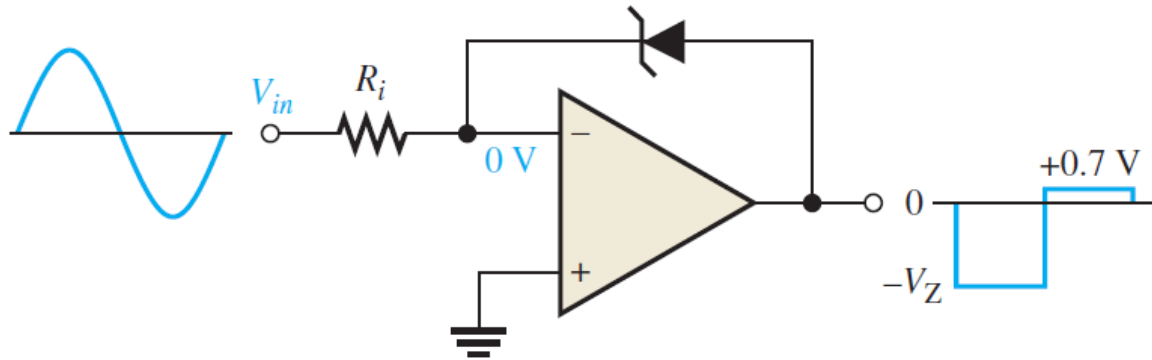
Fig. 17-(b) Bounded at a negative value

Two zener diode connected back to back with a comparator as in Fig. 18 to limit the output voltage to the zener voltage plus the voltage drop (0.7V) of the forward bias zener diode, both positively and negatively.
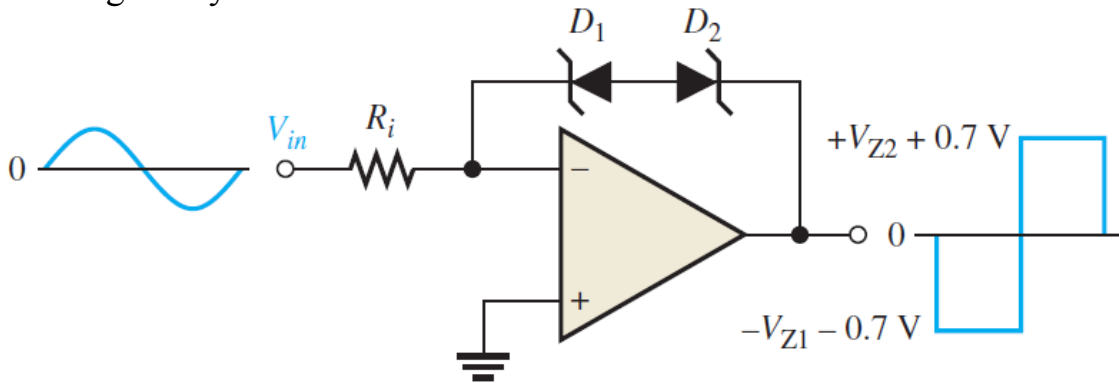
Fig. 18

9- Logarithmic and Antilog Amplifier

Log and antilog amplifiers are used in applications that require compression of analog input data, linearization of transducers that have exponential outputs, and analog multiplication and division. They are often used in high-frequency communication systems, including fiber optics, for processing wide dynamic range signals.

Note: The **logarithm** of a number is the power to which the base must be raised to get that number. A logarithmic (log) amplifier produces an output that is proportional to the logarithm of the input, and an antilogarithmic (antilog) amplifier takes the antilog or inverse log of the input.

a- Logarithmic Amplifier

The logarithmic amplifier is the use of a feedback-loop device that has an exponential terminal characteristic curve (diode or BJT transistor) which is characterized by

$$ I_D = I_R(e^{V_D/V_T} - 1) \approx I_R e^{V_D/V_T} \qquad \text{.......(1)} $$

Where I_R is reverse leakage current, I_D is the forward diode current, V_D is the forward diode voltage (approximately 0.7 V), V_T is the thermal voltage and is a constant equal to approximately 25 mV at 25C°.

12
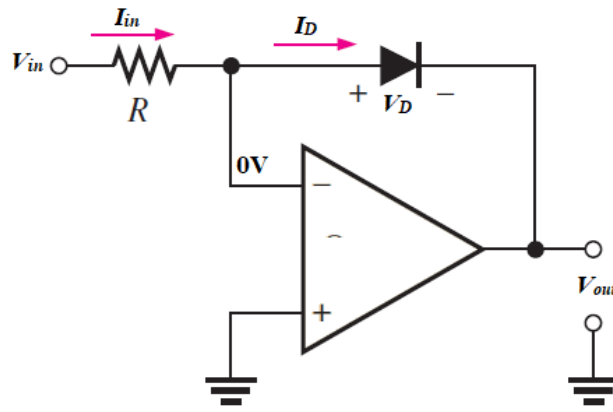
Fig. 19

An analysis of the circuit in Figure 19 is as follows, beginning with the facts that:

$$I_{in} = \frac{V_{in}}{R} = I_D \quad \ldots\ldots\ldots(2)$$

and $\quad V_D = -V_o \quad \ldots\ldots\ldots(3)$

Substituting into the formula of eq. 1,

$$\frac{V_{in}}{R} = I_R e^{-V_{out}/V_T} \quad \rightrightarrows \quad V_{in} = RI_R e^{-V_{out}/V_T}$$

Take the natural logarithm (ln) of both sides

$$\ln(V_{in}) = \ln(RI_R e^{-V_{out}/V_T}) \Rightarrow \ln(V_{in}) = \ln(RI_R) - \frac{V_{out}}{V_T} \quad \ldots\ldots(4)$$

$$V_{out} = V_T[\ln(RI_R) - \ln(V_{in})] = -V_T \ln\frac{V_{in}}{RI_R} \quad \ldots\ldots(5)$$

Under the condition that the term RI_R is negligible (which can be accomplished by controlling R so that $RI_R \approx 1$, where the factor, I_R, is a constant for a given diode), then gives $V_{out} \approx -V_T \ln(V_{in})$. **Note:** ln is the natural logarithm to the base e. A **natural logarithm** is the exponent to which the base e must be raised in order to equal a given quantity. Although eq. 5 will use natural logarithms in the formulas, each expression can be converted to a logarithm to the base 10(log10) using the relationship $\ln x = 2.3 \log10x$.

Example: Determine the output voltage for the log amplifier in Fig. 19. Assume $I_R = 50$nA and R=100k.

Solution:

$$V_{OUT} = -(0.025 \text{ V})\ln\left(\frac{V_{in}}{I_R R}\right) = -(0.025 \text{ V})\ln\left(\frac{2 \text{ V}}{(50 \text{ nA})(100 \text{ k}\Omega)}\right)$$

$$= -(0.025 \text{ V})\ln(400) = -(0.025 \text{ V})(5.99) = -\mathbf{0.150 \text{ V}}$$

Note1: The output voltage of the logarithmic amplifier is limited to a maximum value of approximately (-0.7V).

Note2: The input must be positive when the diode is connected in the direction shown in the Fig. 19. To handle negative inputs, the diode must be reversed.

Log Amplifier with a BJT

The base-emitter junction of a bipolar junction transistor exhibits the same type of logarithmic characteristic as a diode because it is also a *pn* junction. A log amplifier with a BJT connected in a common-base form in the feedback loop is shown in Figure 20. Notice that *Vout* with respect to ground is equal to $-V_{BE}$.
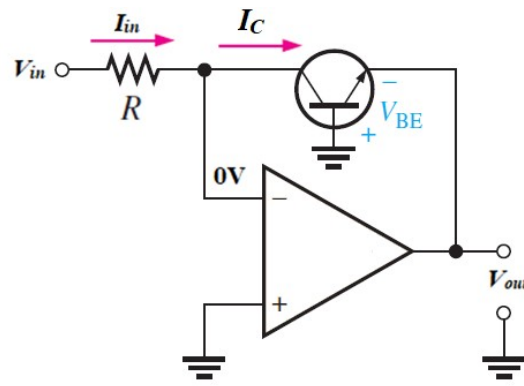
Fig. 20

The analysis for this circuit is the same as for the diode log amplifier except that V_{BE} replaces V_D, I_C replaces I_D and I_{BEO} replaces I_R. The expression for the V_{BE} versus I_C characteristic curve is

$$I_C = I_{EBO}e^{V_{BE}/V_T}$$

where I_{EBO} is the emitter-to-base leakage current. The expression for the output voltage is

$$V_{out} = -V_T \ln(\frac{V_{in}}{I_{EBO}R})$$

b- Antilog Amplifier

The **antilogarithm** of a number is the result obtained when the base is raised to a power equal to the logarithm of that number. To get the antilogarithm, you must take the exponential of the logarithm (antilogarithm of $x=e^{lnx}$).

An antilog amplifier is formed by connecting a transistor (or diode) as the input element as shown in Fig. 21. The exponential formula still applies to the base-emitter *pn* junction. The output voltage is determined by the current (equal to the collector current) through the feedback resistor.

$$Vout = -R_f I_C$$

The characteristic equation of the *pn* junction is

$$I_C = I_{EBO}e^{V_{BE}/V_T}$$

Substituting into the equation for V_{out}

$$V_{out} = -R_f I_{EBO}e^{V_{BE}/V_T}$$

As you can see in Fig. 21, $V_{in} = V_{BE}$

$$V_{out} = -R_f I_{EBO}e^{V_{in}/V_T}$$

The exponential term can be expressed as an antilogarithm as follows:

$$V_{out} = -R_f I_{EBO} anti\log(\frac{V_{in}}{V_T})$$

Where V_T is approximately 25 mV.

Fig. 21

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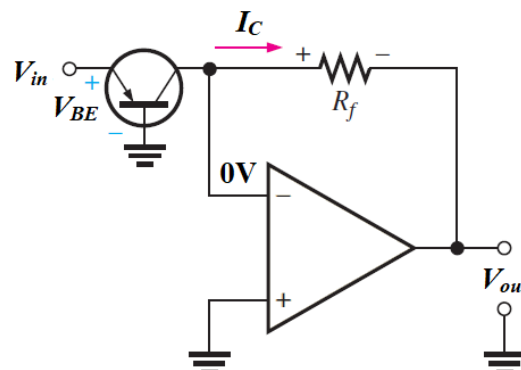
Example: For the antilog amplifier in Figure 21, find the output voltage. Assume $I_{EBO} = 40$ nA, $V_{in}=175.1$ mV and Rf= 68k.

solution

$$V_{out} = -R_f I_{EBO}\text{antilog}\left(\frac{V_{in}}{25 \text{ mV}}\right) = -(68 \text{ k}\Omega)(40 \text{ nA})\text{antilog}\left(\frac{175.1 \text{ mV}}{25 \text{ mV}}\right)$$

$$= -(68 \text{ k}\Omega)(40 \text{ nA})(1101) = -3 \text{ V}$$

Note: In certain applications, a signal may be too large in magnitude for a particular system to handle. In these cases, the signal voltage must be scaled down by a process called **signal compression** so that it can be properly handled by the system. If a linear circuit is used to scale a signal down in amplitude, the lower voltages are reduced by the same percentage as the higher voltages. Linear signal compression often results in the lower voltages becoming obscured by noise and difficult to accurately distinguish, as illustrated in Fig. 22-a. To overcome this problem, a signal with a large dynamic range can be compressed using a logarithmic response, as shown in Figure 22-b. In logarithmic signal compression, the higher voltages are reduced by a greater percentage than the lower voltages, thus keeping the lower voltage signals from being lost in noise.
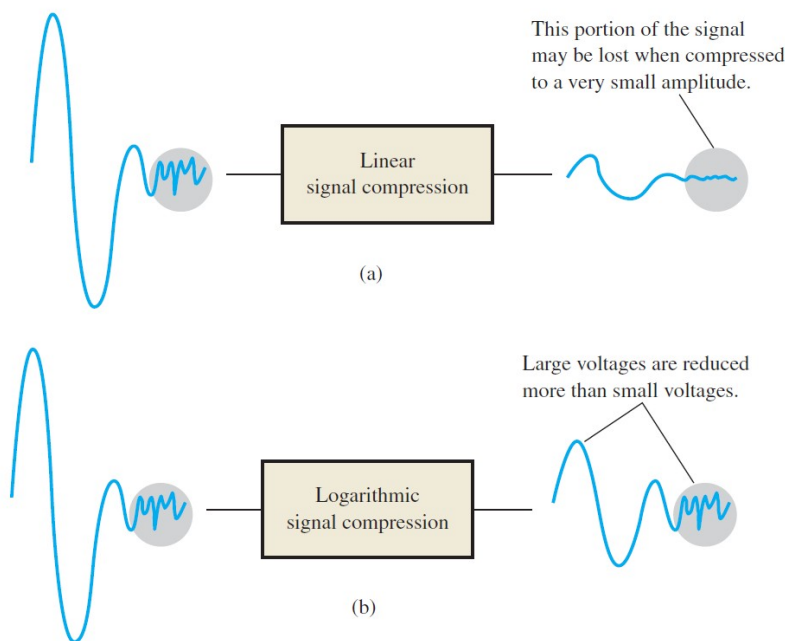
Fig. 22

+++
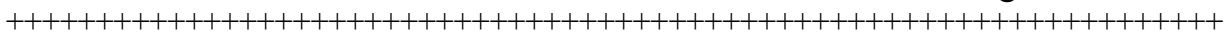
Questions

1. What purpose does the diode or transistor perform in the feedback loop of a log amplifier?
2. Why is the output of a log amplifier limited to about 0.7 V?
3. What are the factors that determine the output voltage of a basic log amplifier?
4. In terms of implementation, how does a basic antilog amplifier differ from a basic log amplifier?
5. Define the term *bounding* in relation to a comparator's output.
6. What is the reference voltage for each comparator in Figure 23?

Fig. 23

15
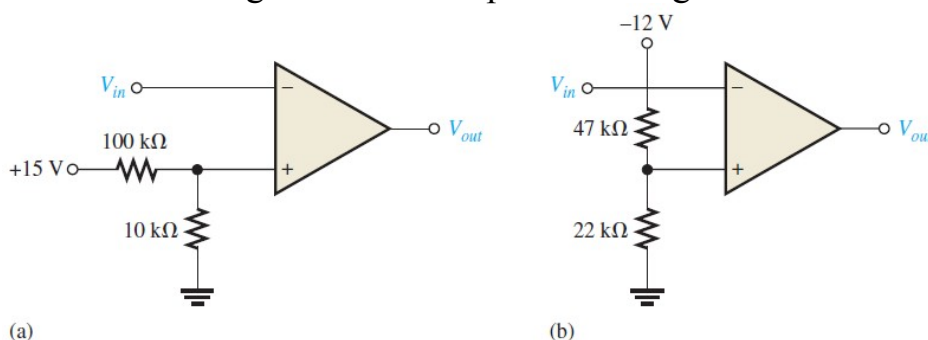
Other OP-AMP Circuts

This section introduces other op-amp circuits that represent basic applications of the op-amp. These circuit, of course, not a comprehensive coverage of all possible op-amp circuits but is intended only to introduce some common basic uses.

1- Constant Current Source

A constant-current source delivers a constant current to the load even the load resistance changes. Figure 24 shows a basic circuit in which a voltage source (V_{IN}) provides a constant current (I_i) through the input resistor (R_i).

Since the inverting input of the op-amp is at virtual ground (0V), the value of (I_i) is determined by

$$I_i = \frac{V_{IN}}{R_i}$$

Now, since $\qquad I_i = I_L$

$$I_L = \frac{V_{IN}}{R_i}$$

If R_L changes, I_L remains constant as long as V_{IN} and R_i are held constant.
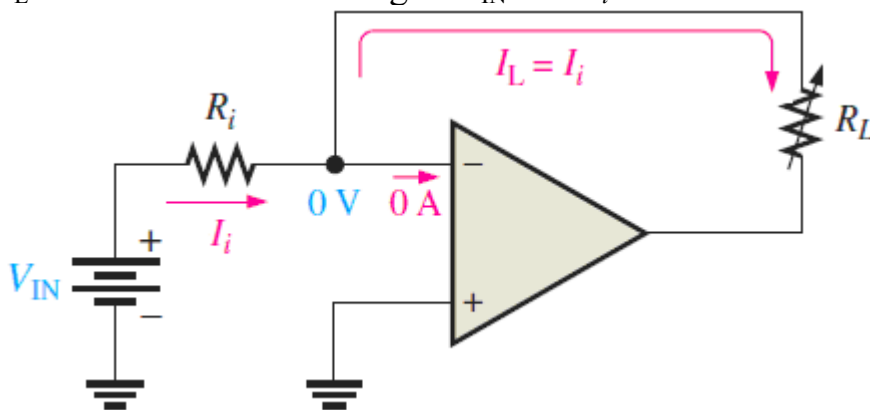
Fig. 24

2- Precision Rectifiers

Rectifier circuits can be implemented with silicon junction diodes. Recall that for the diode to conduct, the voltage across it must be ≈ 0.7 V. Therefore, a major limitation of these circuits is that they cannot rectify voltages below about 0.7 V. In addition, since the input voltage has to rise to about 0.7 V before any appreciable change can be seen at the output, the output is distorted as shown in Fig. 25.

The output of a half- wave rectifier is distorted due to real diode characteristics
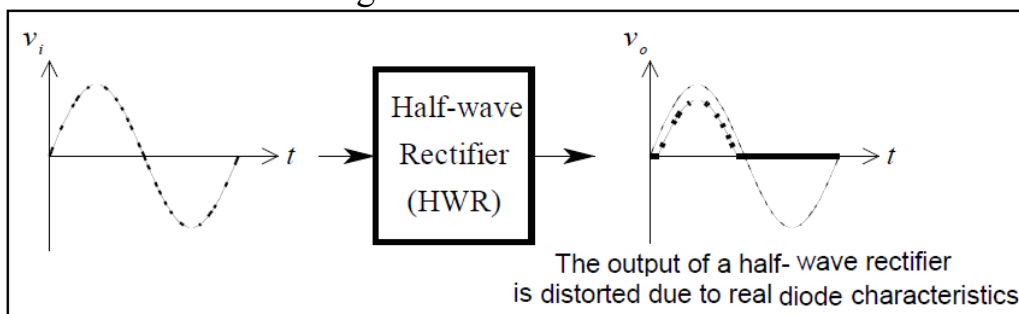
Fig. 25

- *half-wave rectifier* (HWR) is a circuit that passes only the positive (or only the negative) portion of a wave, while blocking out the other portion. The transfer characteristic of the positive HWR is:

$v_O = v_i$ for $v_i > 0$, $v_O = 0$ for $v_i < 0$.

- *full-wave rectifier* (FWR), besides passing the positive portion, inverts and then passes also the negative portion. Its transfer characteristic is:

$v_O = v_i$ for $v_i > 0$, $v_O = v_i$ for $v_i < 0$. or, more concisely, $v_O = |v_i|$

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i- Half-Wave Rectifiers

Figure 26 below shows a precision half-wave rectifier circuit consisting of a diode placed in the negative-feedback path of an ideal op-amp.
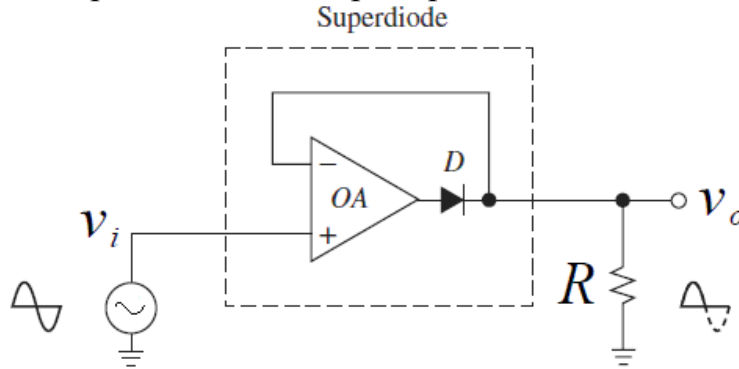
Fig. 26

The analysis of the circuit of Fig. 26 above is illustrated as below:

1- when input voltage is positive $(v_i > 0)$, the op-amp output (v) will also positive, turning ON the diode and thus creating the negative-feedback path shown in Fig. 27-a. This allows op amp to operate as voltage follower and give $v_o = v_i$ (prove that). The output of the op amp (v) is a diode drop above v_O, $(v = v_O + V_{D(on)}) \approx v_O + 0.7$ V.

2- when input voltage is negative $(v_i < 0)$: The op amp output (v) is negative, turning the diode OFF and thus causing the current through R to go to zero. Hence, $v_O = 0$. As shown in Fig. 27-b, the op amp is now operating in the open-loop mode.

(a)   (b)
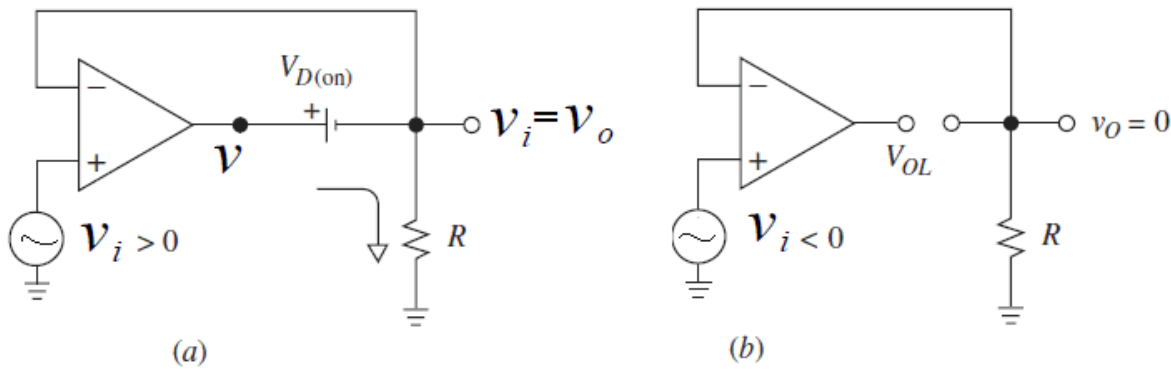
Fig. 27

A disadvantage of this circuit is that when v_i changes from positive to negative the op-amp will be saturated close to its negative supply rail. Thus, the op amp output may exhibit intolerable distortion. The improved HWR of Fig. 28 alleviates this inconvenience by using a second diode. Circuit operation is summarized as:

1- $v_i > 0 \Rightarrow v_O = 0$. (positive input causes D_1 to conduct, thus creating a negative-feedback path around the op amp. By the virtual-ground, D_1 now clamps the op amp output at $v = -V_{D1(on)} \approx -0.7$ V. Moreover, D_2 is OFF, so no current flows through R_2 and, hence, $v_O = 0$).

2- $v_i < 0 \Rightarrow v_O = v_i$. (negative input causes the op amp output positive, thus turning D_2 ON. This creates an alternative negative-feedback path via D_2 and R_2. Clearly, D_1 is now OFF, so the op amp operate as inverting amplifier, i.e. $v_O = (-R_2/R_1)v_i$).

Fig. 28

17
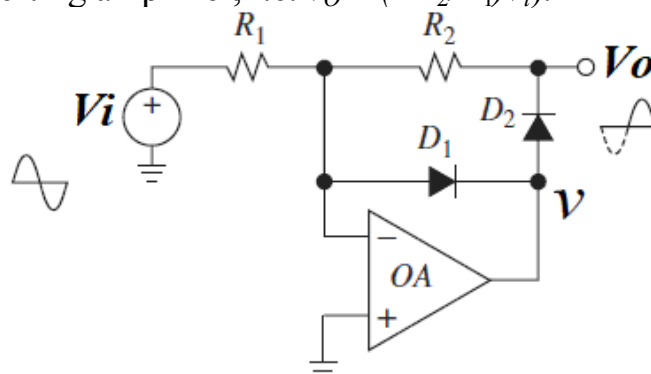
Full-Wave Rectifiers

There are many configuration for achieving precision FWR. One of them is given in Fig. 29. Here op amp (OA1) provides inverting half-wave rectification, and op amp (OA2) sums v_i and the HWR output (v_{HW}) to give $v_O = -[(R_5/R_4)v_i + (R_5/R_3)v_{HW}]$.

Where $v_{HW} = -(R_2/R_1)v_i$ for $v_i > 0$, and $v_{HW} = 0$ for $v_i < 0$.

Fig. 29

18
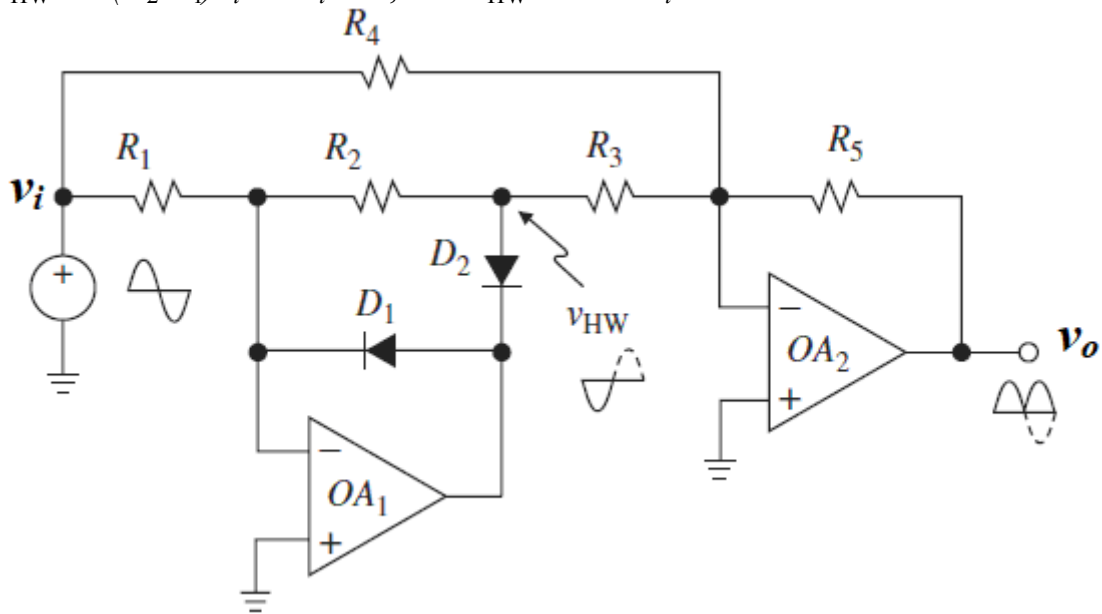
Example1: Draw the output showing its proper relationship to the input signal of the comparator circuit shown in Fig.30. Assume the maximum output levels of the op-amp are ± 12V.
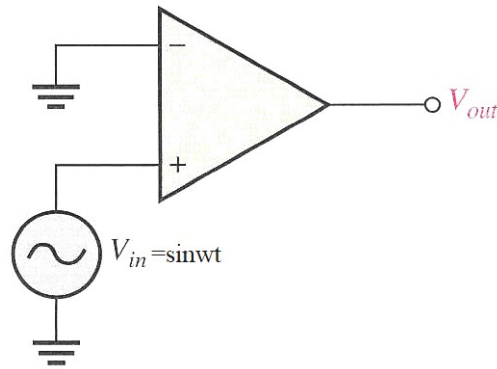
Fig.30

Solution:
When Vin > 0 ⊐ Vout =+12 (maximum positive level)
When Vin > 0 ⊐ Vout =-12 (maximum negative level)
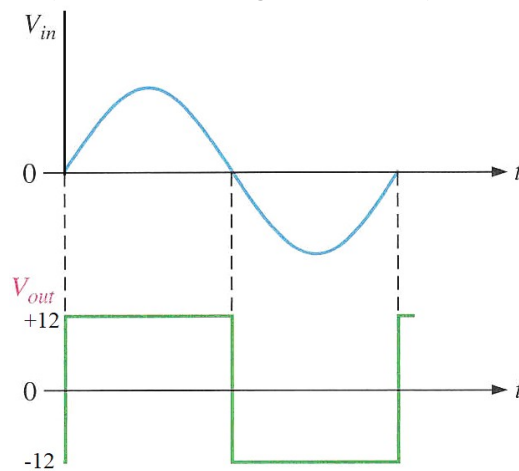
Fig. 40

Example2: Draw the output showing its proper relationship to the input signal of the comparator circuit shown in Fig.41. Assume the maximum output levels of the op-amp are ±12V.
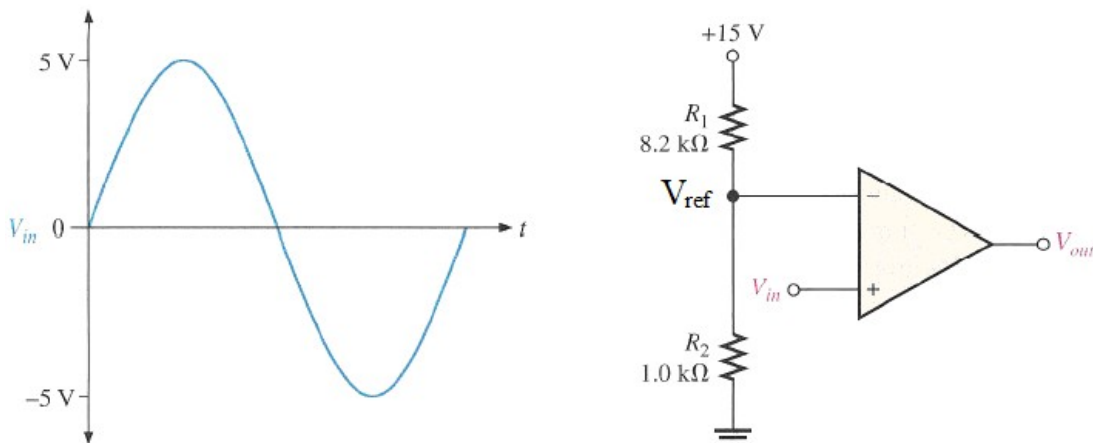
Fig.41

Solution:
The reference voltage (V_{REF}) is set by R_1 and R_2 (use voltage divider rule)

$$V_{REF} = \frac{R_2}{R_1 + R_2}(+V) = \frac{1.0\ k\Omega}{8.2\ k\Omega + 1.0\ k\Omega}(+15\ V) = 1.63\ V$$

As shown in Fig. 42, each time the input exceeds +1.63 V, the output voltage switches to its +12V level, and each time the input goes below +1.63 V, the output voltage switches to its -12V level.

19
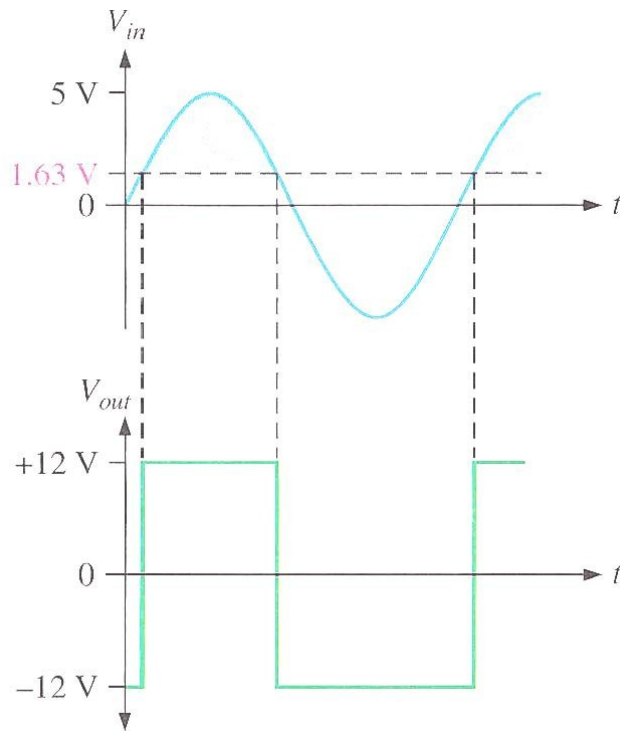
Fig. 42

Problem: Draw the output showing its proper relationship to the input signal of the comparator circuits shown in Fig.43. Assume the maximum output levels of the op-amp are ± 15V.
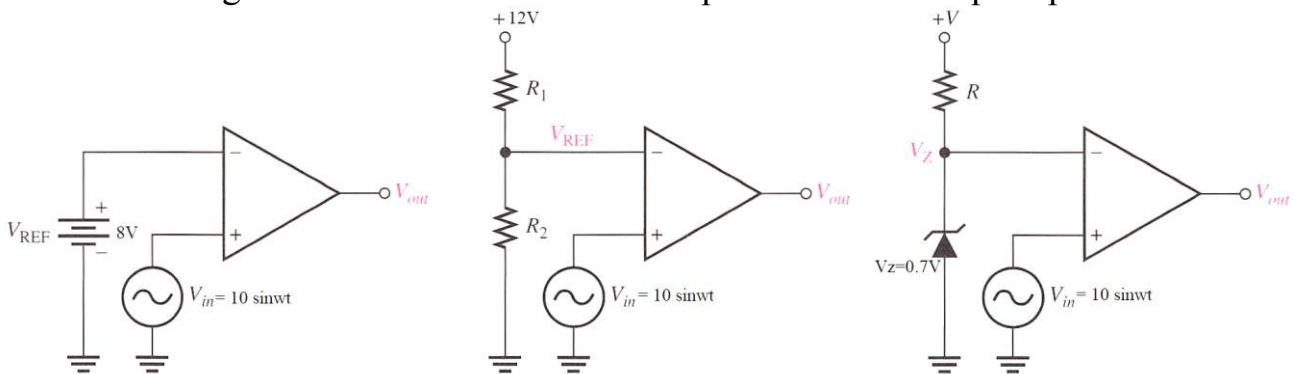
Fig. 43

Example3: Determine the output voltage response to the input square wave for the ideal integrator in Fig. 44. The output voltage is initially zero.
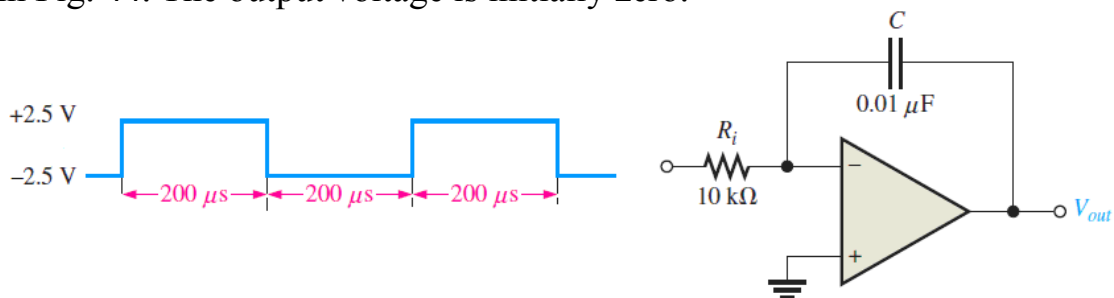
Fig. 44

Solution

The output voltage during the time that the input is at +2.5 V (capacitor charging) is

The output voltage during the time that the input is negative (capacitor discharging) is the same as during charging except it is positive.

When the input is at +2.5 V, the output is a negative-going ramp. When the input is at -2.5V the output is a positive-going ramp.

During the time the input is at +2.5 V, the output is a negative-going ramp (will go from 0 to -5). During the time the input is at -2.5V the output is a positive-going ramp (will go from -5 V to 0 V). Therefore, the output is a triangular wave with peaks at 0 and -5 as shown in Fig. 45.
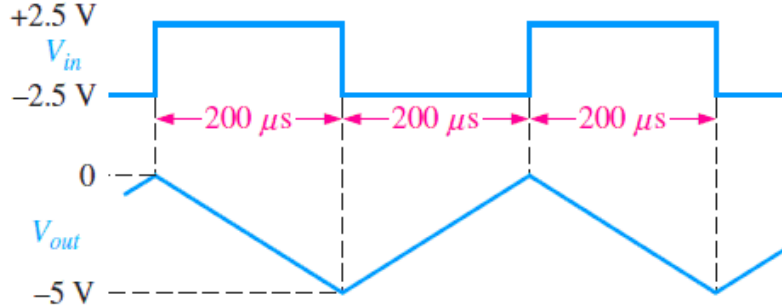
Fig. 45

Example: Determine the output voltage of the ideal op-amp differentiator in Fig.46 for the triangular-wave input shown.
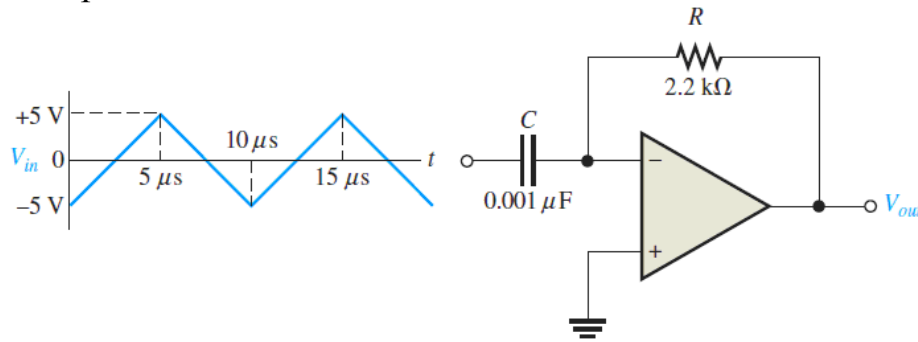
Fig.46

Solution

Starting at $t=0$, the input voltage is a positive-going ramp ranging from -5V to +5V (+10V change) in 5μs. Then it changes to a negative-going ramp ranging is:

$$\text{Time constant} = R\,C = (2.2\ k\Omega)\,(0.001\ \mu F) = 2.2\ \mu s$$

And

$$\frac{dV_{in}}{dt} = \frac{\Delta V_{in}}{\Delta t} = \frac{(-5-5)V}{(5-0)\ \mu s} = 2V/\mu s$$

$$V_{out} = -RC\frac{dV_{in}}{dt} = -2.2\times 2 = -4.4V$$

Likewise, the slope of the negative-going ramp is -2V/μs and the output voltage is

$$V_{out} = -(-2.2\times 2) = 4.4V$$

Figure 47 shows a graph of the output voltage waveform relative to the input.

Fig. 47

21
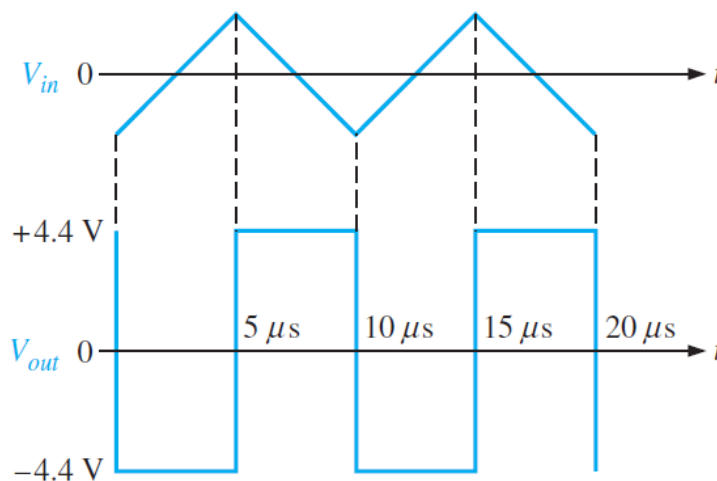
ex:- Draw the output voltage of the integrator
if the input voltage is square wave with
1KHZ frequency and 10pp.p. ($R = 10K\Omega$, $C = 0.1\mu f$)

Solution :- $f = 1 KHZ \Rightarrow t = \dfrac{1}{f} = \dfrac{1}{1000} = 1 ms$

* for positive half cycle $U_{in} = +5$ Volt

$$U_0 = -\dfrac{1}{RC}\int_0^{0.5ms} U_{in}\,dt = -\dfrac{1}{RC}\int_0^{0.5ms} 5\,dt = -\dfrac{5}{RC}\,t\Big|_0^{0.5} = \dfrac{-5 * (0.5)}{10*10^3 * 0.1*10^{-6}}$$

$= -2.5 V$

[(-2.5V) ما رقيمة طرفية جزء المجية عند طاقة لتولتية ايان]

* for negative half cycle , $U_{in} = -5$ Volt

$\therefore U_0 = 2.5 V$

[(2.5V) ما رقيمة طرفية الجزء السالب من طاقة لتولتية ايان]
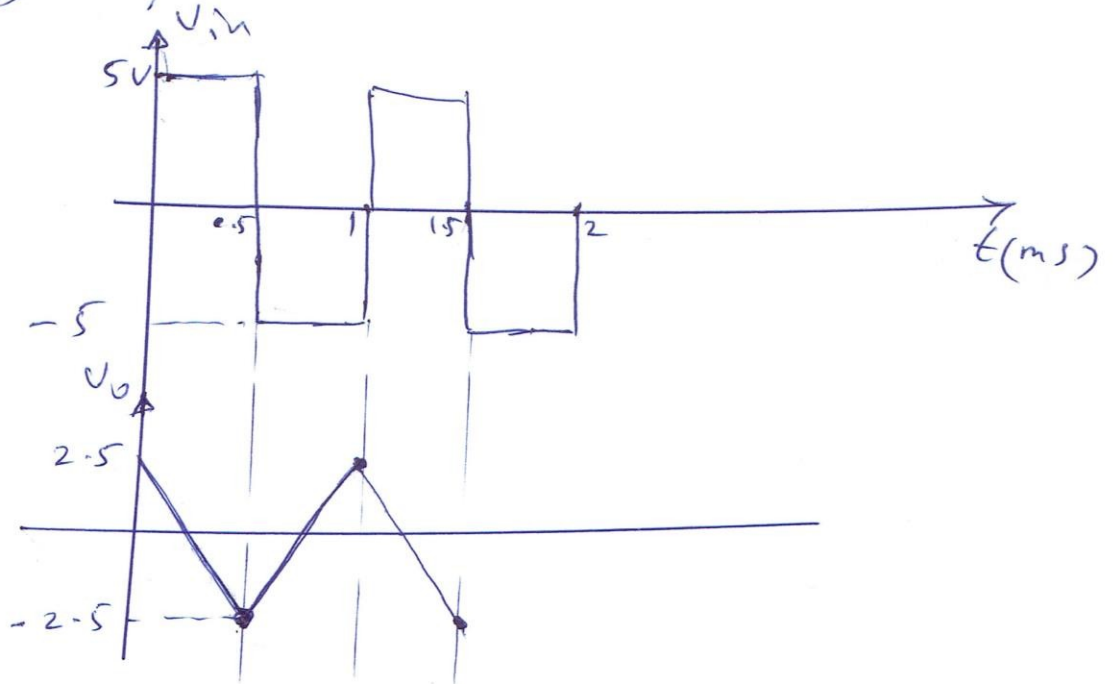
ex② Draw the output voltage of the differentiator
if the input voltage is given in Fig.a, and
the freq. is 1KHZ $(R = 10K, C = 0.1Mf)$

Solution:- $f = 1KHZ \implies t = \dfrac{1}{10^{10}} = 1ms$

Fig.a.

$A \rightarrow B$

$\dfrac{dV_{in}}{dt} = \dfrac{\Delta V_{in}}{\Delta t} = \dfrac{2-0}{0.5-0} = 4 \times 10^3 \, V/s$

$U_0 = -RC \dfrac{dV_{in}}{dt} = -10 \times 10^3 \times 0.1 \times 10^{-6} \times 4 \times 10^3$

$= -4V$

$B \rightarrow C$

$\dfrac{dV_{in}}{dt} = \dfrac{\Delta V_{in}}{\Delta t} = \dfrac{0-2}{1-0.5} = -4 \times 10^3 \, V/s$

$U_0 = 4V$
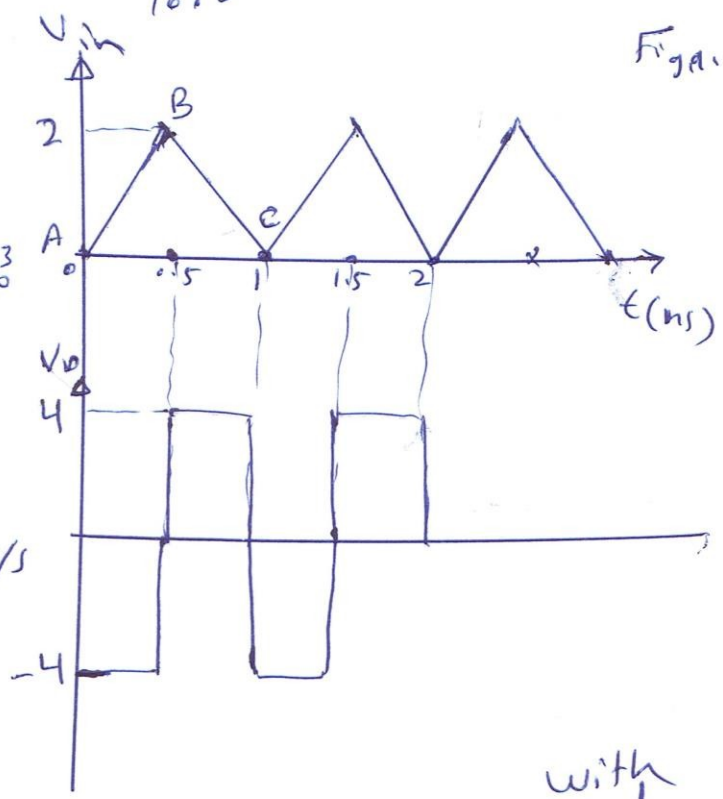
This means that the
output voltage is a square wave with 4Up with and
the same freq. of the input voltage

23

ex.③ Design a circuit with help of op-amp that give output $(U_0 = 10\sin t - 2\cos t)$ if the input voltage is $(U_{in} = 2\sin t)$. (assume $RC = 1$)
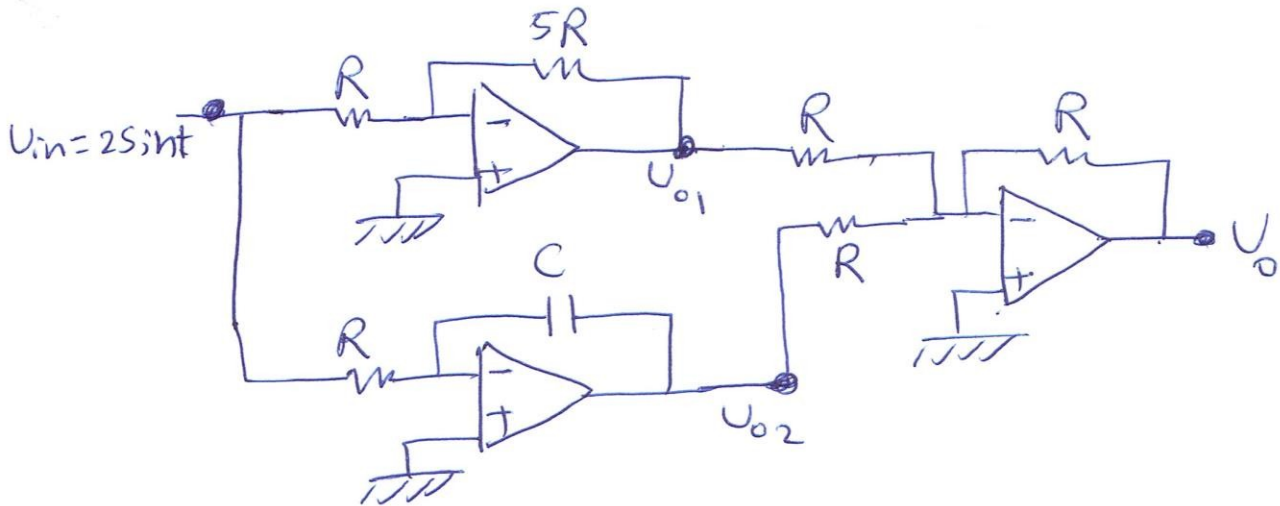
$$U_{01} = \frac{-5R}{R} * 2\sin t = -10\sin t$$

$$U_{02} = -\frac{1}{RC}\int U_{in}\,dt = -1\int 2\sin t\,dt = 2\cos t$$

$$U_0 = -(U_{01} + U_{02}) = -(-10\sin t + 2\cos t) = \boxed{10\sin t - 2\cos t}$$

ex.④ what is the output of this circuit $(V_{sat} = \pm 13)$
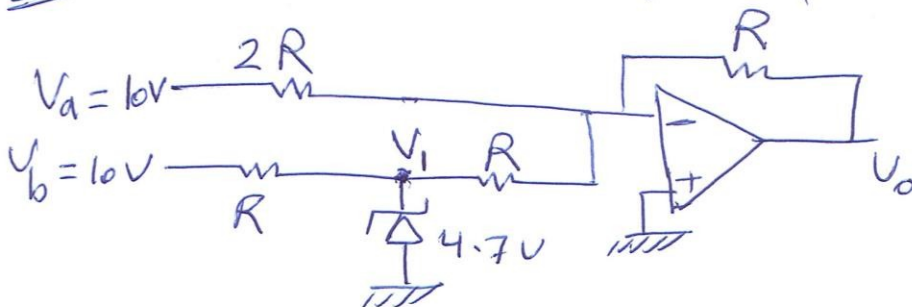
Solution:- $U_1 = 4.7\,V$

$$U_0 = -\left(\frac{R}{R}U_1 + \frac{R}{2R} \times 10\right) = -(4.7 + 5) = -9.7\,Volt$$

problem : repeat ex. 4 if

① $V_b = 3$ volt

② all resistances have the same values (with $V_b = 10$?

③ Zener diode is reversed $(V_b = 3V)$ ($V_b = 3V$)

ex 5 := for the circuit shown in figs., find the relation of the output voltage

① V_1
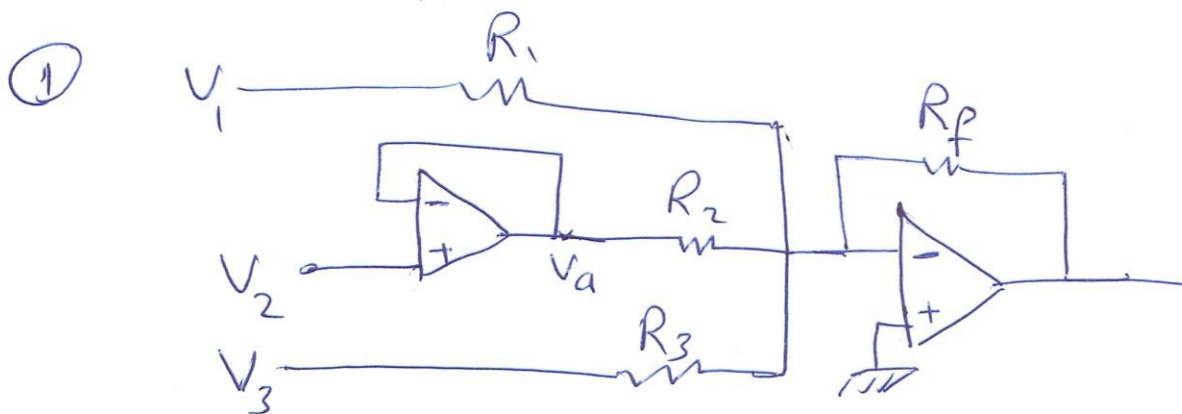
$$U_a = V_2 \quad (\text{voltage follower})$$

$$U_0 = -\left(\frac{R_f}{R_1} U_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} U_3 \right)$$
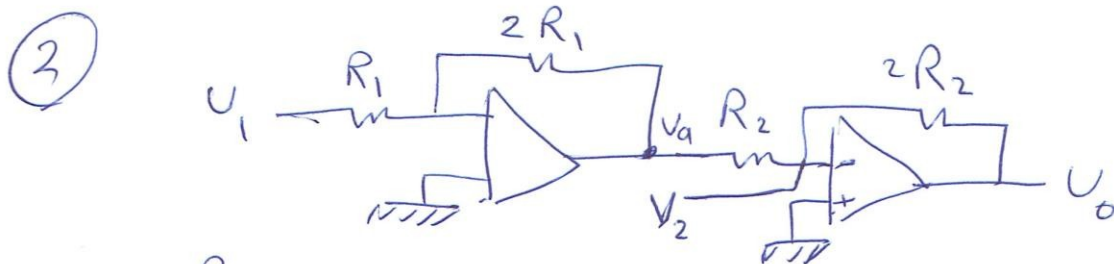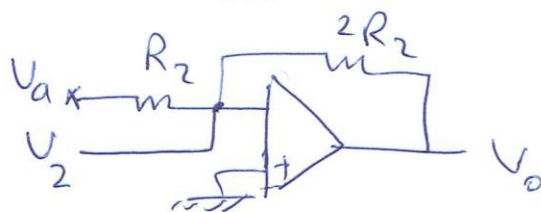
②

$$U_a = \frac{-2R_1}{R_1} U_1 = -2 U_1$$

$$\frac{V_a - V_2}{R_2} = \frac{V_2 - V_0}{2R_2} \Rightarrow V_a - V_2 = 0.5 V_2 - 0.5 U_0 \Rightarrow 0.5 V_0 = 1.5 V_2 - V_a$$

$$\therefore U_0 = 3 V_2 - 2 V_a \Rightarrow \boxed{V_0 = 3V_2 + 4V_1}$$

ex 6 Desigen Circuit to solve the following
differential equation

$$f(t) = \frac{d^2V}{dt^2} + 10\frac{dU}{dt} + 2V$$

Solution

نرتب المعادلة بحيث تكون أعلى مشتقة بالطرف الأيسر

$$\frac{d^2V}{dt^2} = -10\frac{dU}{dt} - 2V + f(t)$$

$$\frac{d^3V}{dt} = -10\frac{dU}{dt} - 2V + f(t)$$
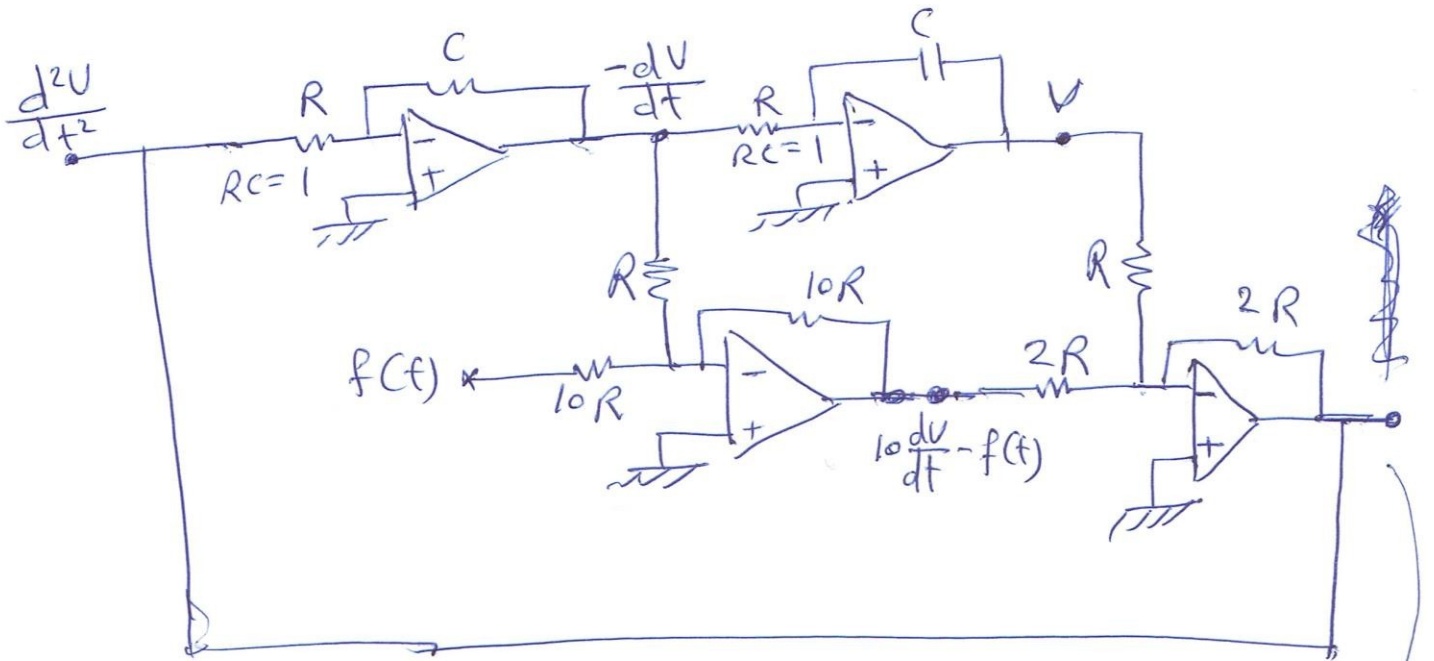
لحل مثل هذه المسألة نأخذ أعلى مشتقة ونعتبرها دخل (i/P) ونعتبرها الثانية ($\frac{d^2V}{dt^2}$) ودمجناها عطينا مشتقة أول ($\frac{dU}{dt}$) ودمجناها للمرة مرة أخرى عطينا مشتقة (V) وبإضافة هذه الحدود إلى الدالة [$f(t)$] مؤشر جامع عطينا أعلى ($\frac{d^2V}{dt^2}$) والذي لشده يمسار تغذية كلية تقفل الدائرة

Digital to Analog conversion

It is an important interface process for converting digital signals to analog signals. An example is a voice signal that is digitized for storage, processing, or transmission and must be changed back into an approximation of the original audio signal in order to drive a speaker. The $R/2R$ ladder is more commonly method used for D/A conversion because it requires only two resistor values as shown in Fig. 48 for four bits.
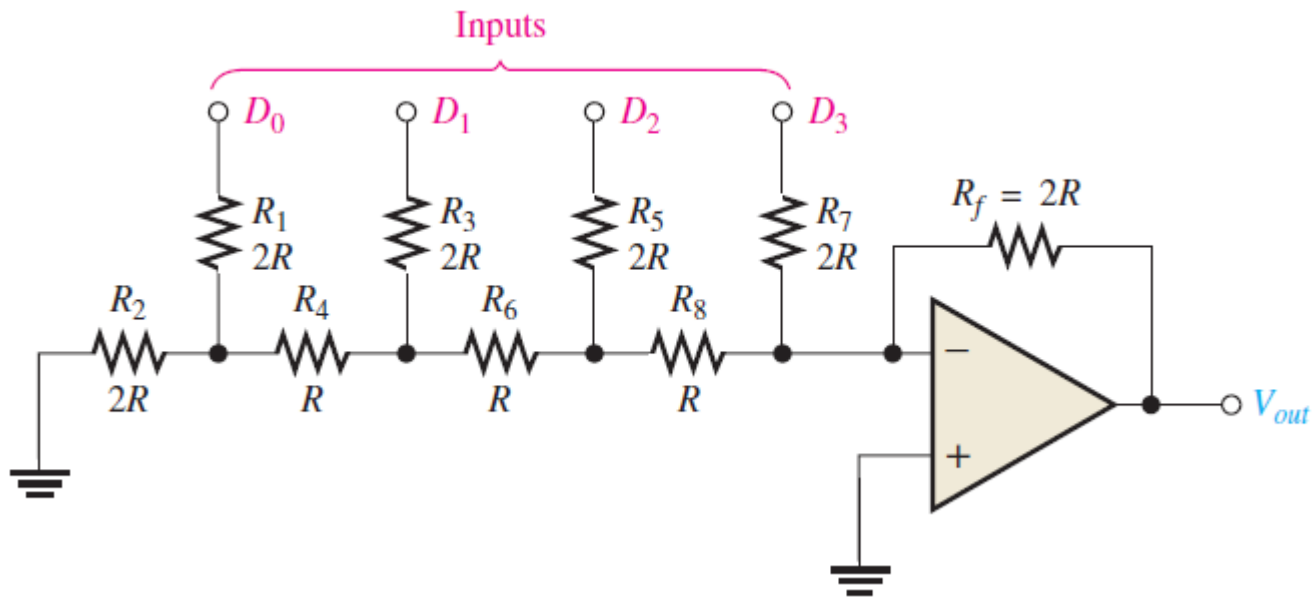

Fig. 48

Assume that the $D3$ input is HIGH (+5 V) and the others are LOW (ground, 0 V). This condition represents the binary number 1000. A circuit analysis will show that this reduces to the equivalent form shown in Fig. 49 (a).

Essentially no current goes through the $2R$ equivalent resistance (R_{EQ}) because the inverting input is at virtual ground. Thus, all of the current ($I=5/2R$) through $R7$ is also through Rf, and the output voltage is -5V.
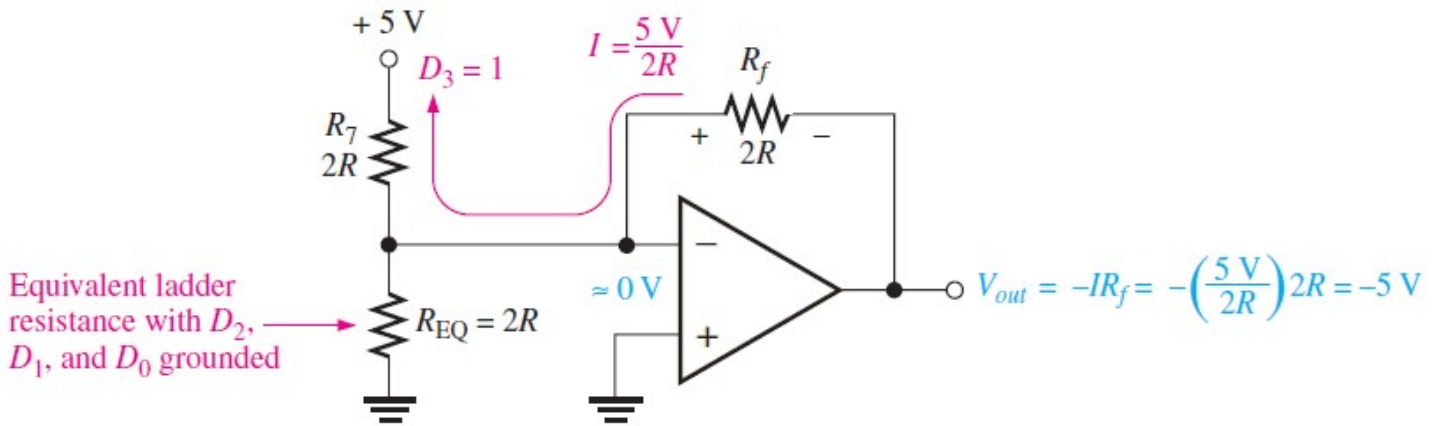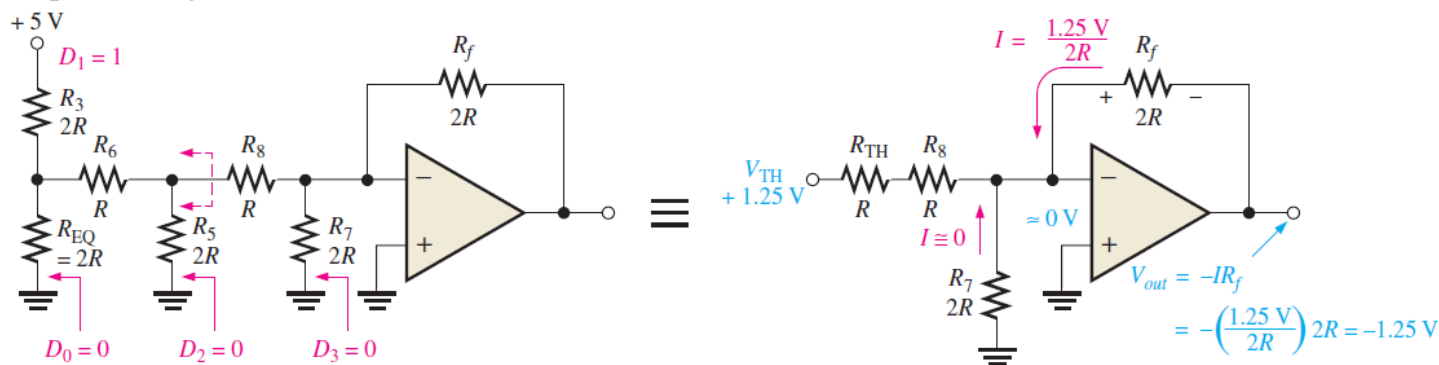

(a) Equivalent circuit for $D_3 = 1$, $D_2 = 0$, $D_1 = 0$, $D_0 = 0$

Figure (b) shows the equivalent circuit when the $D2$ input is at +5 V and the others are at ground. This condition represents 0100. If we thevenize looking from $R8$, we get 2.5 V in series with R, as shown. This results in a current through Rf of $I= 2.5/2R$, which gives an output voltage of -2.5V. Keep in mind that there is no current from the op-amp inverting input and that there is no current through $R7$ because it has 0 V across it, due to the virtual ground.
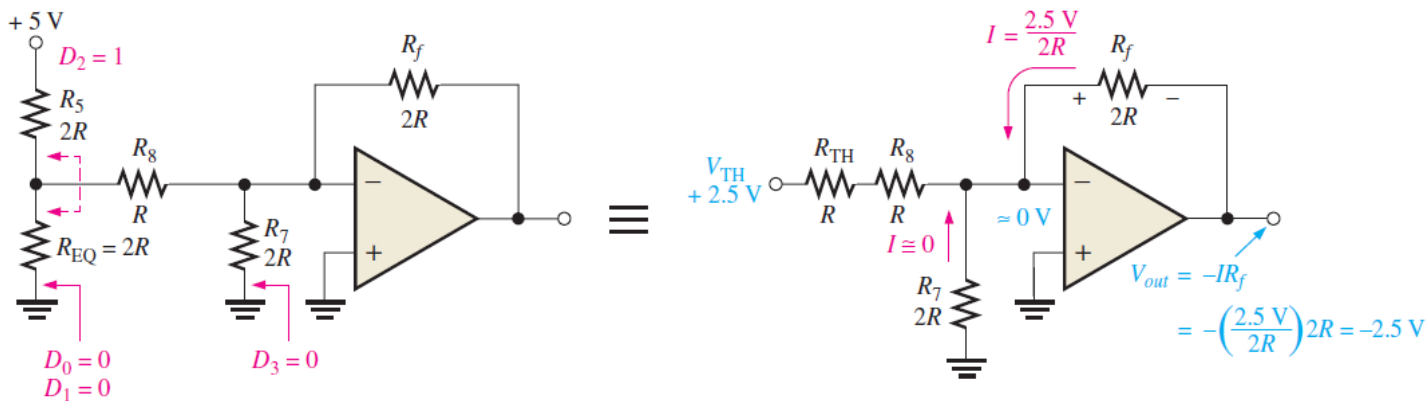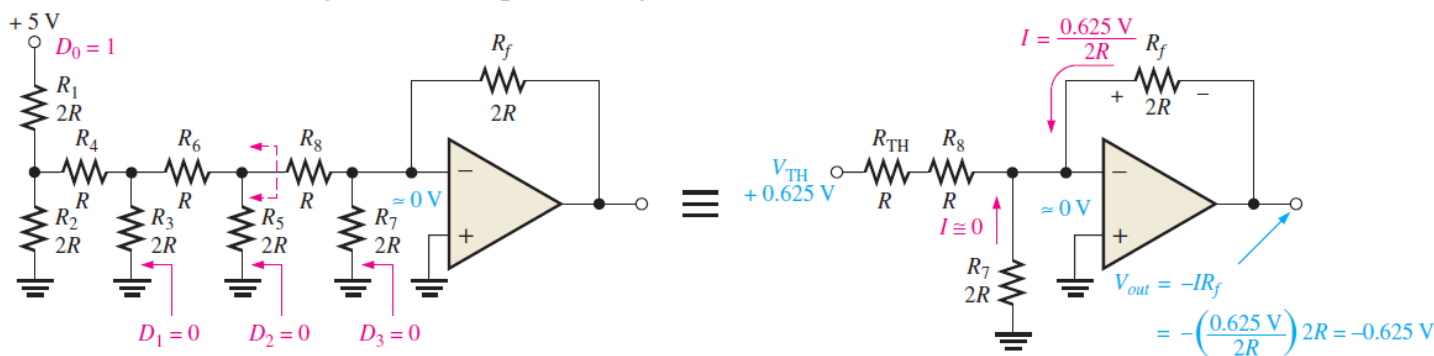
(b) Equivalent circuit for $D_3 = 0$, $D_2 = 1$, $D_1 = 0$, $D_0 = 0$

Figure (c) shows the equivalent circuit when the $D1$ input is at +5 V and the others are at ground. This condition represents 0010. Again thevenizing looking from $R8$, you get 1.25 V in series with R as shown. This results in a current through Rf of $I= 1.25$ V/2R, which gives an output voltage of -1.25.

(c) Equivalent circuit for $D_3 = 0$, $D_2 = 0$, $D_1 = 1$, $D_0 = 0$

In Fig. (d), the equivalent circuit representing the case where $D0$ is at +5 V and the other inputs are at ground is shown. This condition represents 0001. Thevenizing from $R8$ gives an equivalent of 0.625 V in series with R as shown. The resulting current through Rf is $I=0.625$V/2R, which gives an output voltage of -0.625 V.

(d) Equivalent circuit for $D_3 = 0$, $D_2 = 0$, $D_1 = 0$, $D_0 = 1$

Notice that each successively lower-weighted input produces an output voltage that is halved, so that the output voltage is proportional to the binary weight of the input bits.
In summary, We can prove that the equivalent analog voltage shown in Fig. 50 below is obtained from the relation:

$$V_{analog} = \frac{V_A + 2V_B + 4V_C + 8V_D + ...}{2^n}$$

((The proof is left as an exercise))
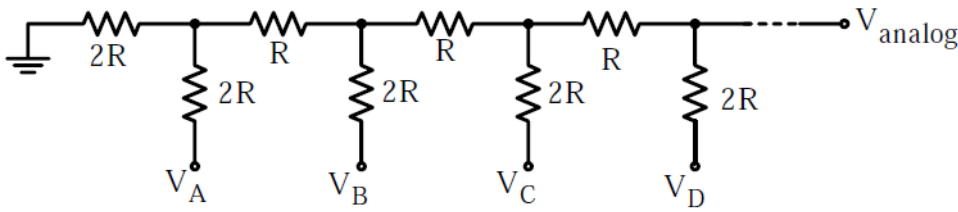
Where (n) is the number of digital inputs.

Fig.50

Figure 51 shows a four−bit R−2R ladder network and an op−amp connected to form a DAC. The op amp shown is an inverting amplifier and in this case the reference voltage (V ref) should be negative so that the amplifier output will be positive. Alternately, a non−inverting op amp could be used with a positive value of (V_{ref})
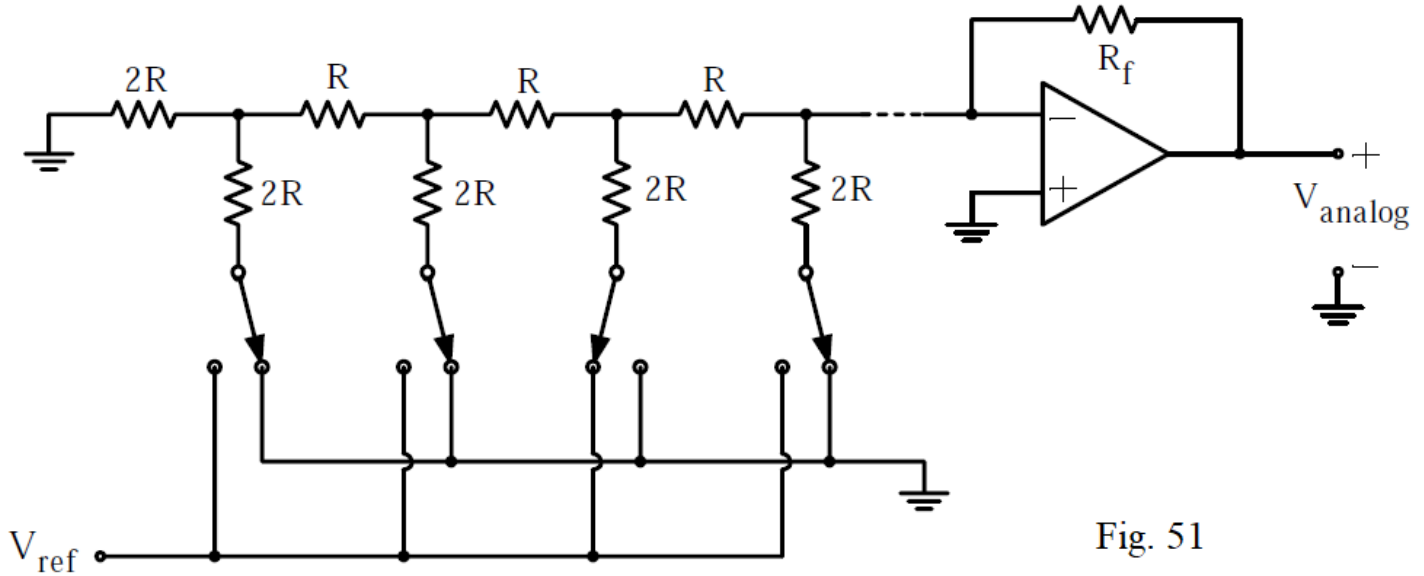

Fig. 51

Example: Figure 52 shows a four−bit DAC where all four switches are set at the ground level. Find the analog voltage value at the output of the unity gain amplifier for each of the sets of the switch positions shown in Table. Fill−in the right−most column with your answers.
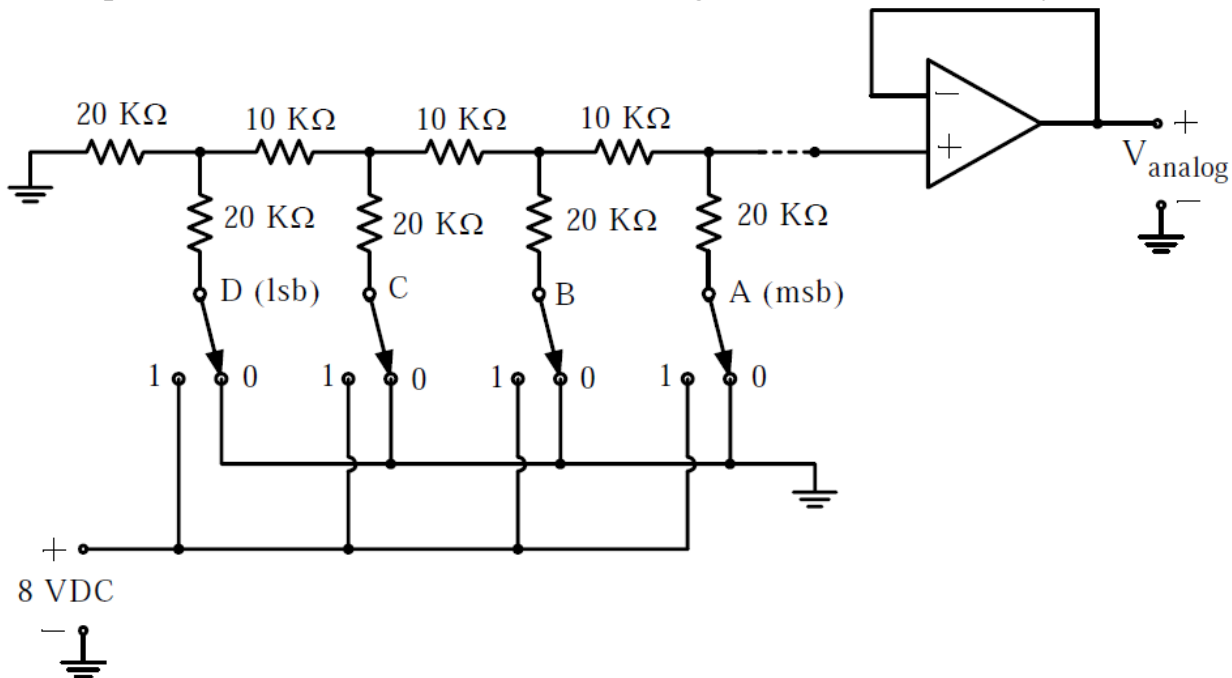
Fig. 52

	A 2^0	B 2^1	C 2^2	D 2^3	
(a)	1	1	1	1	
(b)	1	0	0	1	
(c)	1	0	1	0	
(d)	0	1	0	0	

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Solution:
This is a 4−bit DAC and thus we have $n=2^4=16$ distinct binary values from 0000 to 1111 corresponding to decimals 0 through 15 respectively.

a. $V_{analog} = \dfrac{V_A + 2V_B + 4V_C + 8V_D}{2^n} = \dfrac{1 \times 8 + 2 \times 8 + 4 \times 8 + 8 \times 8}{2^4} = 7.5 \text{ V}$

b. $V_{analog} = \dfrac{V_A + 2V_B + 4V_C + 8V_D}{2^n} = \dfrac{1 \times 8 + 2 \times 0 + 4 \times 0 + 8 \times 8}{2^4} = 4.5 \text{ V}$

c. $V_{analog} = \dfrac{V_A + 2V_B + 4V_C + 8V_D}{2^n} = \dfrac{1 \times 8 + 2 \times 0 + 4 \times 8 + 8 \times 0}{2^4} = 2.5 \text{ V}$

d. $V_{analog} = \dfrac{V_A + 2V_B + 4V_C + 8V_D}{2^n} = \dfrac{1 \times 0 + 2 \times 8 + 4 \times 0 + 8 \times 0}{2^4} = 1.0 \text{ V}$

Based on these results, we can now fill−in the right−most column with the values we obtained, and we can plot the output versus inputs of the R−2R network for the voltage levels and as shown in Figure 53.
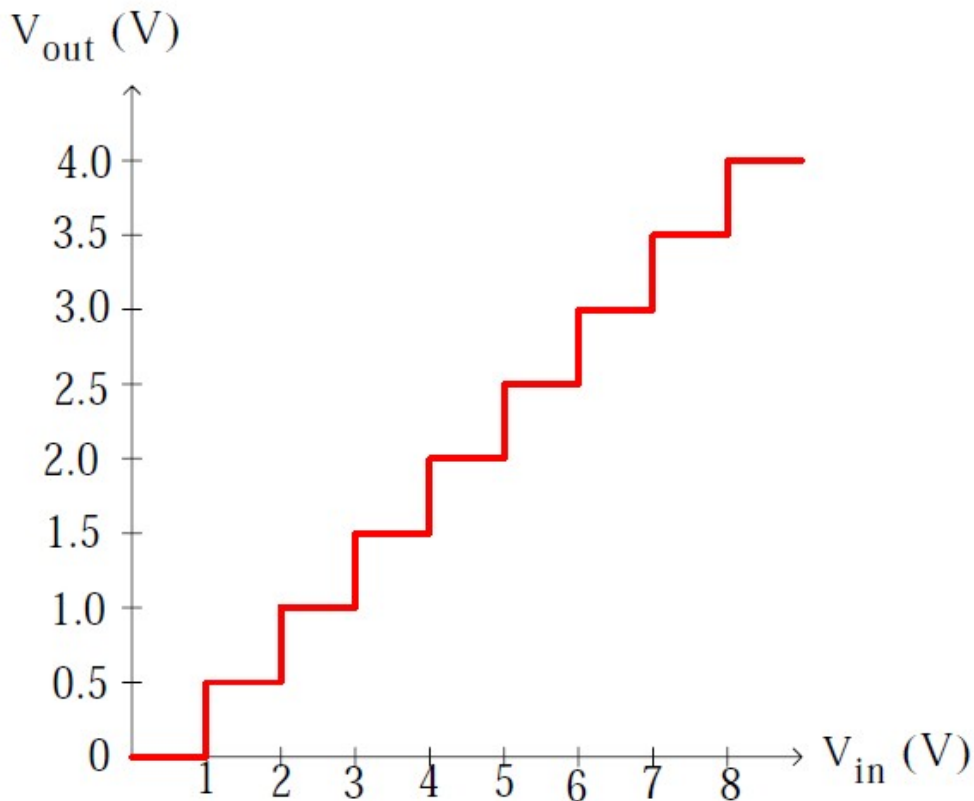

Fig.53

Active Filters

A filter circuit can be constructed using passive components like resistors and capacitors. But an active filter, in addition to the passive components makes use of an *OP-AMP* as an amplifier. The amplifier in the active filter circuit may provide voltage amplification and signal isolation or buffering. There are four major types of filters namely, low-pass filter, high-pass filter, and band-pass filter and band-stop filter. All these four types of filters are discussed in the following sections.

1- ***low−pass filter*** transmits (passes) all frequencies from dc or zero frequency up to a *critical* (*cutoff*) frequency denoted as w_c, and *attenuates* (blocks) all frequencies above this cutoff frequency. An op amp low−pass filter is shown in Figure 54(a &b) and its amplitude frequency response in Figure 54(c).

In Figure 54(c), the blue lines represent the ideal characteristics and the smooth curve represents the practical characteristics, where the gain does not reduce immediately to zero. The vertical scale represents the magnitude of the ratio of output to input voltage V_{out}/V_{in}, that is, the gain A_v.

The cutoff frequency w_c is the frequency at which the maximum value of V_{out}/V_{in} falls to $0.707C_v$, and this is called the *half power* or the -3dB point.
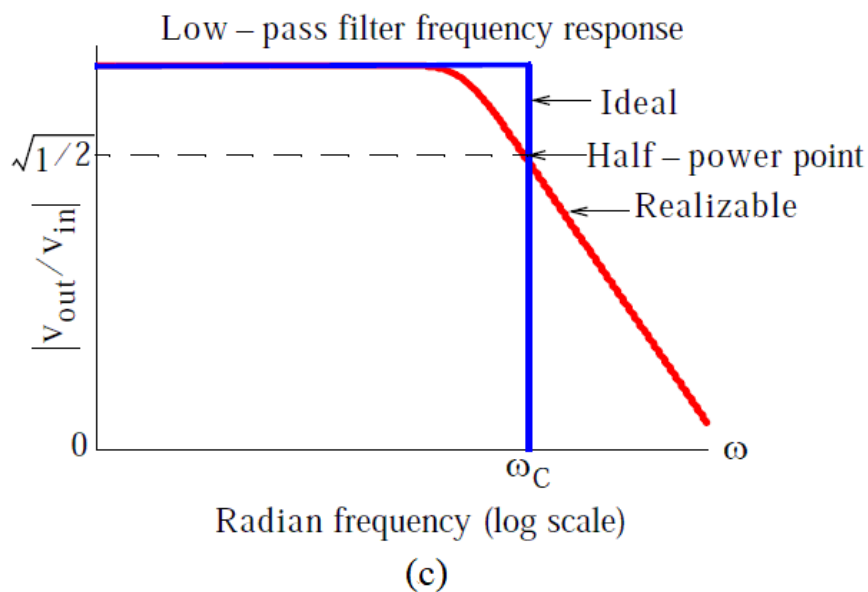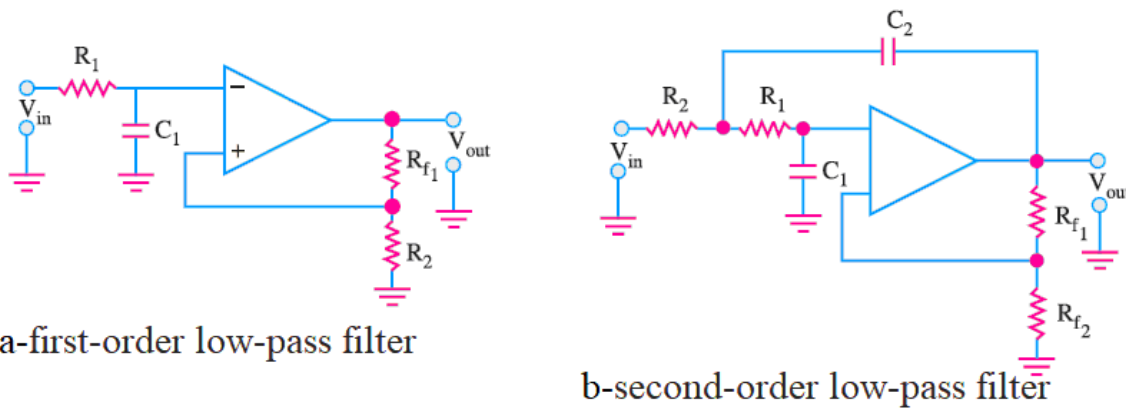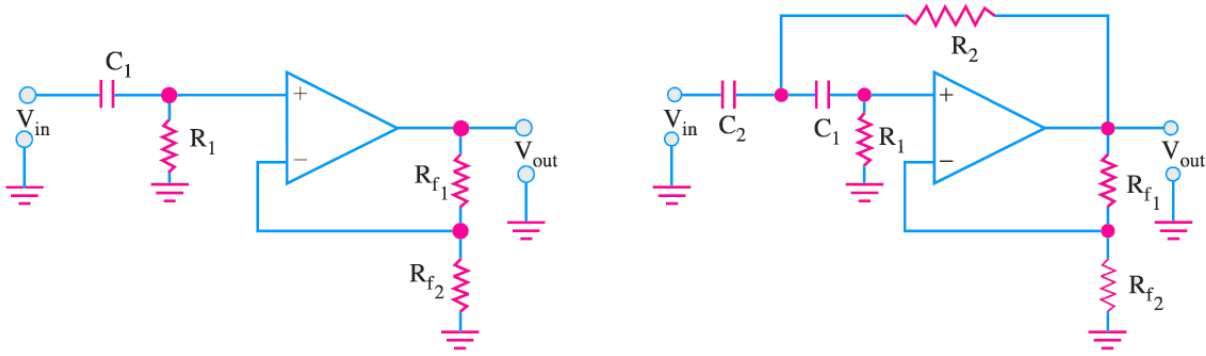

a-first-order low-pass filter

b-second-order low-pass filter

(c)

Figure 5 4. An active low−pass filter and its amplitude frequency response

2- ***high−pass filter*** passes all frequencies above a cutoff frequency w_c , and blocks all frequencies below the cutoff frequency. An op amp high−pass filter is shown in Figure 55(a&b) and its frequency response in Figure 55(c).

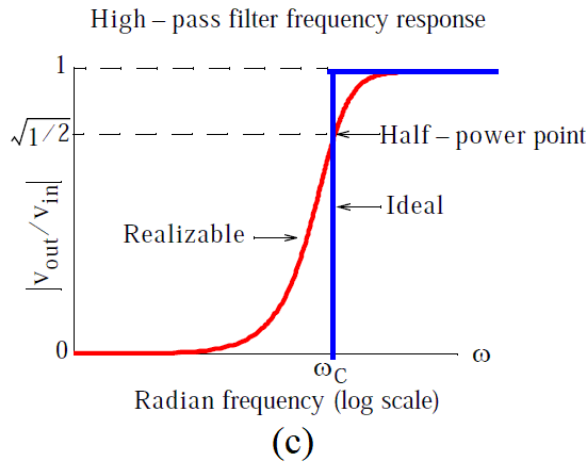(a) first order high-pass filter   (b) second-order high-pass filter.

(c)

Figure 5 5. An active high–pass filter and its amplitude frequency response

3- **band−pass** **filter** passes the band (range) of frequencies between the cutoff frequencies denoted as w_1 and w_2, where the maximum value of A_v which is unity, falls to $0.707C_v$, while it blocks all frequencies outside this band. A simple way to construct a band-pass filter is to cascade a low-pass filters and a high-pass filter as shown in Figure 56(a) and its frequency response in Figure 56(b). The values of w_1 and w_2 can be obtained by using the relations, $1/R_1C_1$ and, $1/R_2C_2$. Then band width,

$$BW = w_2 - w_1$$
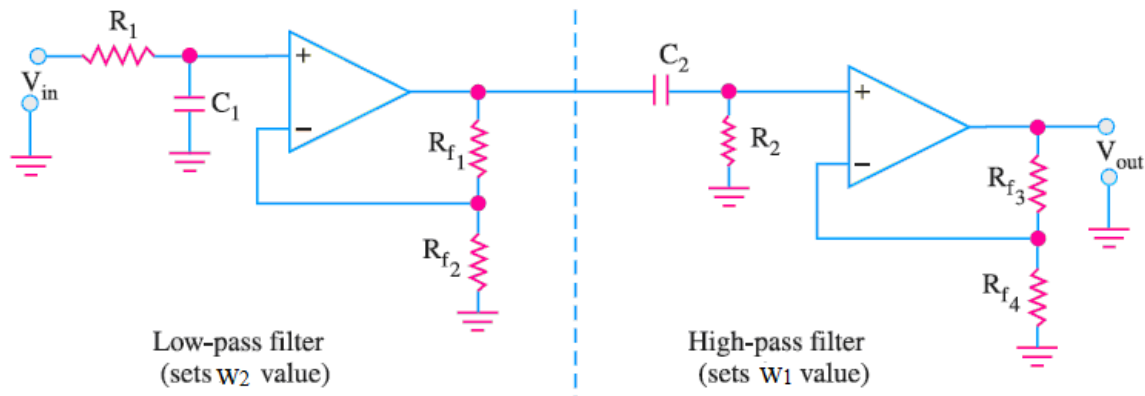
And the centre frequency,

$W_0 = w_1w_2$

The Quality-factor (or *Q*-factor) of the band pass filter circuit.

Q=W0/BW

Low-pass filter
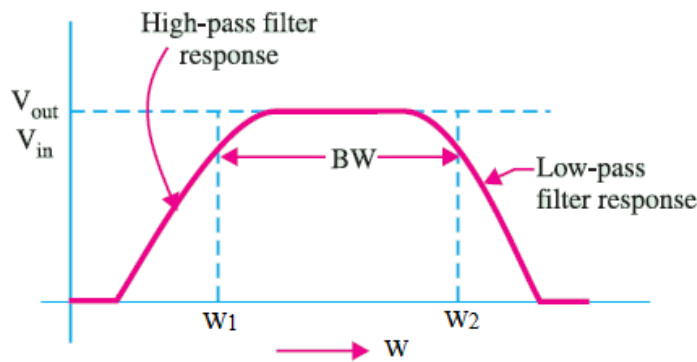(sets w2 value)

High-pass filter
(sets w1 value)

Fig 56

4- **band−elimination** or **band−stop** or **band−rejection** **filter** attenuates (rejects) the band of frequencies between the critical (cutoff) frequencies denoted as w_1 and w_2, where the maximum value of C_v which is unity, falls to $0.707C_v$, while it passes all frequencies outside this band. An op amp band−stop filter is shown in Figure 57(a) and its frequency response in Figure 57(b). The block diagram shows that the circuit is made up of a high-pass filter, a low-pass filter and a summing amplifier. The summing amplifier produces an output that is equal to a sum of the filter output voltages. The circuit is designed in such a way so that the cut-off frequency, $w1$ (which is set by a low-pass filter) is lower in value than the cut-off frequency, $w2$ (which is set by high-pass filter). The gap between the values of $w1$ and $w2$ is the bandwidth of the filter. When the circuit input frequency is lower than $w1$, the input signal will pass through low-pass filter to the summing amplifier. Since the input frequency is below the cut-off frequency of the high pass filter, V2 will be zero. Thus the output from the summing amplifier will equal the output from the low-pass filter. When the circuit input frequency is higher than $w2$, the input signal will pass through the high-pass filter to the summing amplifier. Since the input frequency is above the cut-off frequency of the low-pass filter, V1 will zero. Now the summing amplifier output will equal the output from the high-pass filter.

(a)

(b)

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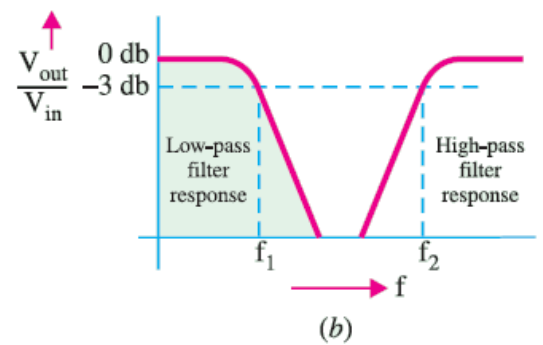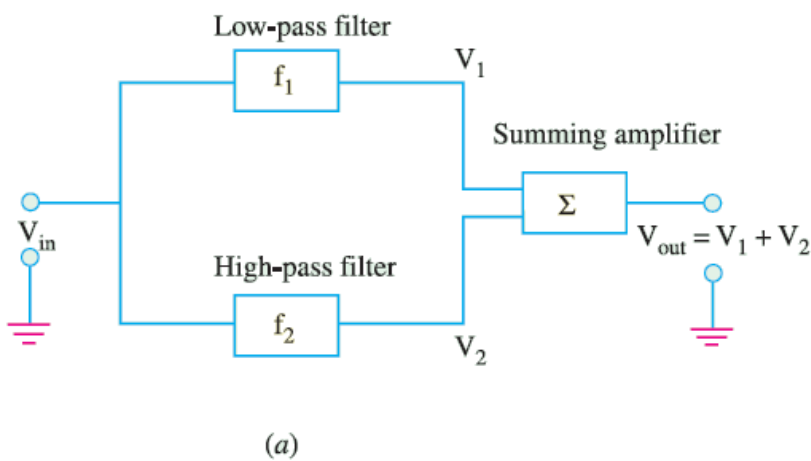
Butterworth Filter

There are many different types of active filters. Among the most useful of them are Butterworth filters because they have an excellent response. Butterworth filters, named after British engineer Stephen Butterworth.

Table-1 below gives the Butterworth polynomials for n up to 8. Note that for n even, the polynomials are the products of quadratic forms, and for n odd, there is present the additional factors (s+1).

NORMALIZED POLYNOMIALS THAT PRODUCE BUTTERWORTH RESPONSES

ORDER	NORMALIZED DENOMINATOR POLYNOMIALS
1	$(s+1)$
2	$(s^2 + 1.414s + 1)$
3	$(s+1)(s^2 + s + 1)$
4	$(s^2 + 0.7654s + 1)(s^2 + 1.848s + 1)$
5	$(s+1)(s^2 + 0.6180s + 1)(s^2 + 1.618s + 1)$
6	$(s^2 + 0.5176s + 1)(s^2 + 1.414s + 1)(s^2 + 1.932s + 1)$
7	$(s + 1)(s^2 + 0.445s + 1)(s^2 + 1.247s + 1)(s^2 + 1.802s + 1)$
8	$(s^2 + 0.390s + 1)(s^2 + 1.111s + 1)(s^2 + 1.663s + 1)(s^2 + 1.962s + 1)$

$$2k = 3 - A_{Vo} \quad \text{or} \quad A_{Vo} = 3 - 2k \quad \text{.......(1)}$$

And
$$\omega_o = \frac{1}{RC}$$

We are now in a position to synthesize even-order Butterworth filters by cascading prototypes of the form shown in Fig. b , using identical R's and C's and selecting the gain A_{Vo} of each operational amplifier to satisfy Eq. (1) and the damping factors from Table 1.

To realize odd-order filters, it is necessary to cascade the first-order filter of Eq. (1) with second-order sections such as indicated in Fig. b . The first-order prototype of Fig. c has the transfer function of Eq. (1) for arbitrary A_{Vo} provided that ω_o is given by Eq. (2) . For example, a third-order But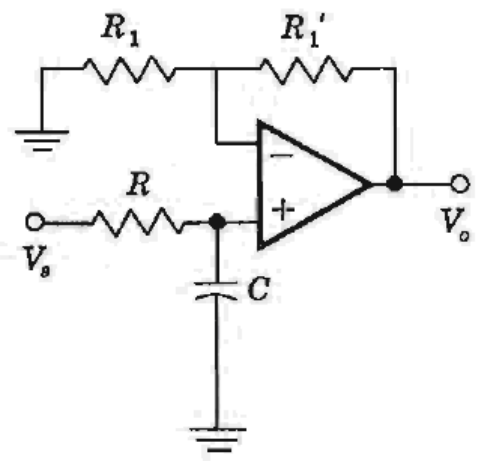terworth active filter consists of the circuit in Fig. b in cascade with the circuit of Fig. c, with R and C chosen so that $RC = 1/\omega_o$.
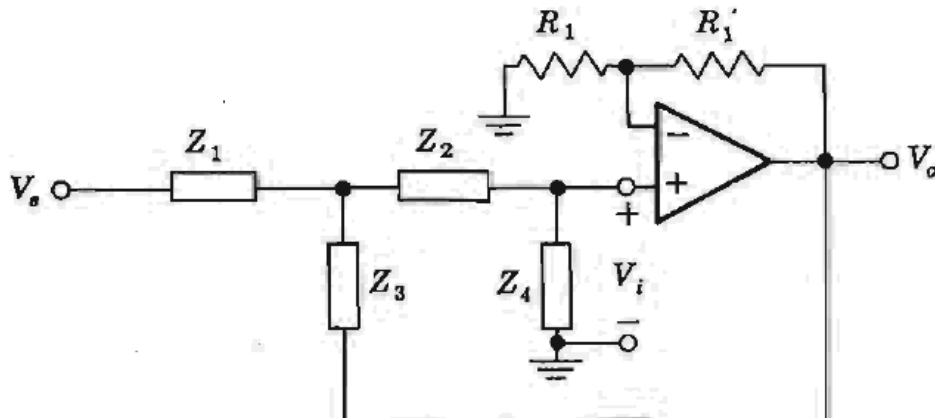
(a) Generalized active-filter prototype.
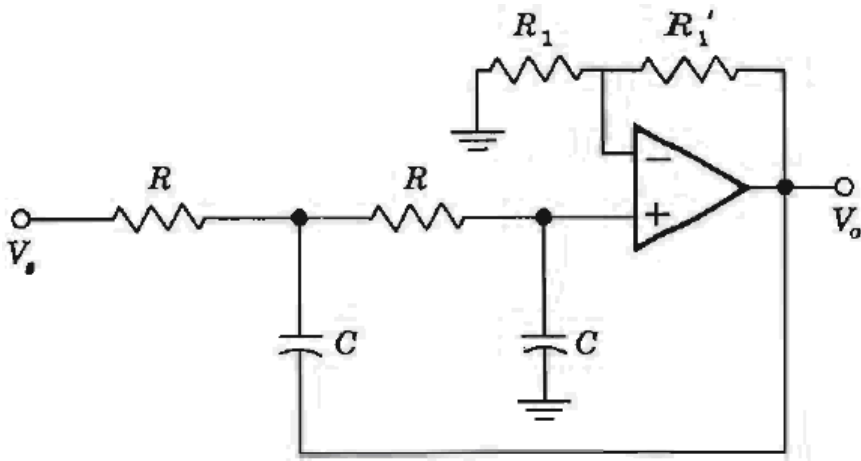
(b) Second-order low-pass section.   (c) First-order low-pass section.

Example: design a fourth-order Butterworth low-pass filter with a cutoff frequency of 1kHz.
Solution
we cascaded two second-order prototypes as given below.

Item	First Stage	Second Stage
Stage parameters	$K_1 = 0.7654$ $f_0 = 1000\,k$	$K_2 = 1.848$ $f_0 = 1000\,k$
Design constraints and Element values	Av1=3-2k1=2.235 Av1= (R1+$\bar{R}$1)/R1 Choose R1= 10k ➔ $\bar{R}$1=12.35 k f_0=1/2πRC ➔ let R=1k ➔ C=0.16uF	Av2=3-2k2=1.152 Av2= (R2+$\bar{R}$2)/R2 Choose R2= 10k ➔ $\bar{R}$2=1.52k f_0=1/2πRC ➔ let R=1k ➔ C=0.16uF

designs Final

Exercise: design a third-order Butterworth low-pass filter with a cutoff frequency of 10kHz.